M. Tech (Electronics-VLSI)(2023-24)

Semester I					**Total Duration: 24 hrs/week** **Total Marks: 500** **Total Credits: 20**				
Subjects	**Teaching Scheme (Hrs) Hrs./Week**		**Examination Scheme (Marks)**						**Credits**
	L	**P**	**Theory**	**Internal Assessment**	**TW**	**PR**	**Oral**	**Total**	
Digital CMOS Design	04	--	50	50	-	--	--	100	04
IC Fabrication	04	--	50	50	-	--	--	100	04
Advanced Digital System Design	04	--	50	50	--	--	--	100	04
Open Elective - I	04	--	50	50	--	--	--	100	04
Lab Practice - I	--	04	--	--	25	--	25	50	02
Lab Practice - II	--	04	--	--	25	--	25	50	02
	16	**8**	**200**	**200**	**50**	--	**50**	**500**	**20**

Semester II					**Total Duration: 24hrs/week** **Total Marks : 500** **Total Credits: 20**				
Subjects	**Teaching Scheme (Hrs) Hrs./Week**		**Examination Scheme (Marks)**						**Credits**
	L	**P**	**Theory**	**Internal Assessment**	**TW**	**PR**	**Oral**	**Total**	
Analog CMOS Design	04	--	50	50	--	--	--	100	04
VLSI Test and Testability	04	--	50	50	--	--	--	100	04
Low Power IC Design	04	--	50	50	--	--	--	100	04
Open Elective - II	04	--	50	50	--	--	--	100	04
Lab Practice - I	--	04	--	--	25	--	25	50	02
Lab Practice - II	--	04	--	--	25	--	25	50	02
Total	**16**	**8**	**200**	**200**	**50**	--	**50**	**500**	**20**

Semester III					**Total Duration: 08 hrs/week** **Total Marks : 250** **Total Credits: 20**				
Subjects	**Teaching Scheme (Hrs) Hrs./Week**		**Examination Scheme (Marks)**						**Credits**
	L	**P**	**Theory**	**Internal Assessment**	**TW**	**PR**	**Oral**	**Total**	
Seminar	--	02	--	--	50	--	50	100	05
Dissertation Stage - I	--	06	--	--	100	--	50	150	15
Total	**--**	**08**	**--**	**--**	**150**	**--**	**100**	**250**	**20**

Semester IV					**Total Duration: 08 hrs/week** **Total Marks: 250** **Total Credits: 20**				
Subjects	**Teaching Scheme (Hrs) Hrs./Week**		**Examination Scheme (Marks)**						**Credits**
	L	**P**	**Theory**	**Internal Assessment**	**TW**	**PR**	**Oral**	**Total**	
Dissertation Stage - II	--	08	--	--	150	--	100	250	20
Total	**--**	**08**	**--**	**--**	**150**	--	**100**	**250**	**20**

List of Open Electives

Open Elective - I	**Open Elective - II**
VLSI Signal Processing	Current Mode Circuit
System on Chip (SoC)	RF Circuit Design

Bharati Vidyapeeth
(Deemed to be University)
College of Engineering, Pune

M. Tech. (Electronics-VLSI), Sem: I
DIGITAL CMOS DESIGN

Teaching Scheme:	**Examination Scheme:**	**Credits Allotted:**
Theory: 04	End Semester Examination (Theory): 50 Marks	Credits: 04
	Internal Assessment (IA): 50 Marks	
	Total:100 Marks	Total Credits: 04

Course Pre-requisites:

The students should have knowledge of

1	Basic Electronics
2	Electronic Devices
3	Switching Theory and Logic Design

Course Objectives:

1	Focus on systematic analysis and design of digital integrated circuits in CMOS technology
2	Enhance problem-solving and creative circuit design techniques.
3	Emphasize the layout design of various digital integrated circuits.
4	Focus on the methodologies and design techniques related to digital integrated circuits.

Course Outcomes: After learning this course students will be able to

1	MOS physics and emerging new CMOS technologies
2	Model the CMOS inverter with optimised power, area, and timing.
3	Executing layout for various digital integrated circuits
4	Implementing CMOS combinational circuit
5	Devise of CMOS sequential circuits and Depict CMOS memory arrays

UNIT – I	**MOS Structure and CMOS Flow**	**(09 Hours)**
	Review of basic MOS structure, V-I Characteristics, MOS as load, Emerging CMOS technologies-FINFETs, Multi-gate transistors, use of Si in VLSI; Sheet resistance of layers, area capacitance of layers, CMOS process flow, latch-up in CMOS inverter, short channel effects	
UNIT– II	**CMOS Inverter and Its Properties**	**(10 Hours)**
	Inverter Properties: static nMOS, CMOS and BiCMOS inverters, design aspect, switching threshold and noise margin concepts and their evaluation, dynamic behavior, power consumption; MOSFET scaling: constant-voltage and constant-field scaling.	

UNIT – III	**CMOS Fabrication and Layout**	**(09 Hours)**
	CMOS Process Technology, N-well, P-well process, Stick diagram for Boolean functions, Optimization using Euler Theorem, Layout Design Rules	
UNIT – IV	**CMOS Combinational Logic**	**(10 Hours)**
	CMOS Combinational Logic: static CMOS design, pass transistor logic, dynamic logic, speed, power, and noise in dynamic logic, cascading dynamic gates, domino logic, driving large capacitive loads, propagation delay models, wiring capacitances	
UNIT – V	**CMOS Sequential Logic and Clocking of Circuits**	**(10 Hours)**
	CMOS Sequential Logic: static latches and registers, MUX based latches, S-R FF, dynamic latches and registers, Clocking of Circuits: Classification of clocking schemes, clock distribution techniques Semiconductor Memories: static RAM; dynamic RAM; ROM, flash memory	

Text Book/ Reference Books:

1. Kang, Sung Mo, Yusuf Leblebici, Kim C. CMOS digital integrated circuits. 4th Edition, MacGraw-Hill, 2019.
2. Neil.H, E.Weste, David Harris and Ayan Banerjee, CMOS VLSI Design: A Circuit and Systems Perspective, Pearson Education, 2011.
3. Jan M.. Rabaey, Anantha P. Chandrakasan, and Borivoje Nikolić. Digital integrated circuits: a design perspective. Pearson Education, Incorporated., 2016.
4. Hodges, David, Horace Jackson, and Resve Saleh. Analysis and design of digital integrated circuits. McGraw-Hill, Inc., 2003.
5. Lin, Ming-Bo. Introduction to VLSI systems: a logic, circuit, and system perspective. CRC press, 2011.
6. Sorab K Gandhi, VLSI Fabrication Principles: Si and GaAs, John Wiley and Sons, 2010.

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College of Engineering, Pune

M. Tech. (Electronics-VLSI), Sem: I
IC FABRICATION

Teaching Scheme:	**Examination Scheme:**	**Credits Allotted:**
Theory: 04	End Semester Examination (Theory): 50 Marks	Credits: 04
	Internal Assessment (IA): 50 Marks	
	Total:100 Marks	Total Credits: 04

Course Pre-requisites:

The students should have knowledge of

1	Basic Electronics
2	Electronic Devices
3	Engineering Chemistry

Course Objectives:

1	Processes involved in semiconductor manufacturing, lithography, and fabrication
2	Model the oxidation growth rate and understand the oxidation process, the process of diffusion, and the ion implantation process.
3	Assembly techniques and packaging of devices

Course Outcomes: After learning this course students will be able to

1	Acquire knowledge about the various fabrication techniques and understand oxidation growth in the field of VLSI
2	Interpret the various lithography techniques.
3	Assay the concepts of diffusion and ion implantation.
4	Acquire knowledge of different types of deposition.
5	Employ the concept of etching and pattern transfer techniques in fabrication.

UNIT– I	**CMOS IC Technology and Oxidation**	**(10Hours)**
	Introduction to VLSI technology: Moore's law, CMOS IC technology, Clean Room types and Standards, Basic device fabrication steps, Physics of Crystal growth, wafer fabrication and basic properties of silicon wafers. Oxidation: Surface passivation using oxidation. Deal-Grove model, types of oxidations and their kinematics	
UNIT–II	**Lithography**	**(09Hours)**
	The Photolithographic Process, Photo mask Fabrication, Comparison between positive and negative photoresists, Exposure Systems, Characteristics of Exposure Systems, E-beam Lithography, X-ray lithography, Optical Lithography, Ion Lithography.	
UNIT– III	**Diffusion and Ion-Implantation**	**(10Hours)**

	Doping Process, Diffusion: Impurity diffusion; solution of diffusion equation, modeling of diffusion phenomena, Technological processes for diffusion, diffusion systems, Ion Implantation: Implantation system, Principles, techniques and applications, removal of implant damage.	
UNIT– IV	**Etching:**	**(09Hours)**
	Etching: Wet etching techniques, selectivity, isotropy and etch bias, common wet etchants, orientation dependent etching effects; Introduction to plasma technology, plasma etch mechanisms, selectivity and profile control plasma etch chemistries for various films, plasma etch system	
UNIT– V	**Deposition and Assembly techniques**	**(10Hours)**
	Epitaxy and thin film deposition: Thermodynamics of vapor phase growth, Chemical Vapor Deposition (CVD), Metal organic CVD (MOCVD), Molecular beam epitaxy (MBE), reaction rate and mass transport limited depositions, atmospheric-pressure CVD (APCVD), Low pressure CVD (LPCVD), equipment's and applications of CVD. Assembly techniques and Packaging of VLSI Devices	

Text Book/ Reference Books:

1. Sze, S.M., VLSI Technology, Tata McGraw-Hill, 2017.
2. R.C. Jaeger, Introduction to Microelectronic Fabrication, Prentice Hall, 2013.
3. Chen, Wai-Kai. VLSI technology. CRC Press, 2003.
4. Ghandhi, Sorab K. VLSI fabrication principles: silicon and gallium arsenide. John Wiley & Sons, 2008.
5. Plummer, James D. Silicon VLSI technology: fundamentals, practice, and modeling. Pearson Education India, 2009.
6. Shacham-Diamand, Yosi, Tetsuya Osaka, Madhav Datta, and Takayuki Ohba, Advanced nanoscale ULSI interconnects: fundamentals and applications. Springer Science & Business Media, 2009.

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College of Engineering, Pune

M. Tech. (Electronics-VLSI), Sem: I
ADVANCED DIGITAL SYSTEM DESIGN

Teaching Scheme:	**Examination Scheme:**	**Credits Allotted:**
Theory: 04	End Semester Examination (Theory): 50 Marks	Credits: 04
	Internal Assessment (IA): 50 Marks	
	Total:100 Marks	Total Credits: 04

Course Pre-requisites:

The students should have knowledge of

1	Electronic Devices
2	Switching Theory and Logic Design

Course Objectives:

1	CMOS technology's focus on the systematic analysis and design of digital system
2	Focus on the methodologies and design techniques related to advanced digital system

Course Outcomes: After learning this course students will be able to

1	Devise the synchronous sequential circuits
2	Expressing advanced design of asynchronous sequential circuit
3	Integrating FSM design using HDL
4	Correlating Synchronous Design using Programmable Devices
5	Integrating to logic and system design using HDL

UNIT – I	**Sequential Circuit Design**	**(09 Hours)**
	Analysis of clocked synchronous sequential circuits and modeling, State diagram, state table, state table assignment and reduction, Design of synchronous sequential circuits design of iterative circuits, ASM chart and realization using ASM	
UNIT– II	**Asynchronous Sequential Circuit Design**	**(10 Hours)**
	Analysis of asynchronous sequential circuit, flow table reduction, races-state assignment, transition table and problems in transition table, Design of asynchronous sequential circuit, Static, dynamic, and essential hazards, data synchronizers, mixed operating mode asynchronous circuits, designing vending machine controller	
UNIT – III	**FSM Design using HDL**	**(09 Hours)**
	Mealy and Moore designs, Implementation, Moore architecture	
	and HDL templates, Mealy architecture, and HDL templates	

UNIT – IV	**Synchronous Design using Programmable Devices**	**(10 Hours)**
	Programming logic device families, designing a synchronous sequential circuit using PLA/PAL, Realization of finite state machine using PLD, FPGA, Xilinx FPGA, coding for FPGAs. Designing with FPGAs: Design flow for FPGAs, prototyping with FPGAs and debugging.	
UNIT – V	**Logic and System Design using HDL**	**(10 Hours)**
	Logic design with HDL, logic design with behavioural models of combinational and sequential logic, synthesis of combinational and sequential logic HDL operators, Arrays, concurrent and sequential statements, packages, different modeling, compilation, and simulation of HDL code, Test bench, realization of combinational and sequential circuits using HDL,Registers, counters, sequential machine, serial adder, Multiplier	

Text Book/ Reference Books:

1. Roth Jr, Charles H., Larry L. Kinney, and Eugene B. John. Fundamentals of logic design.
Cengage Learning, 2020.
2. Ciletti, Michael D. Advanced digital design with the Verilog HDL. Vol. 1. Upper SaddleRiver: Prentice Hall, 2003.
3. Astola, Jaakko, and Radomir S. Stankovic. Fundamentals of switching theory and logic design.
Heidelberg: Springer, 2006.
4. Brown, Stephen D., and Zvonko G. Vranesic. Fundamentals of digital logic with Verilog
design. Vol. 1. New York: McGraw-Hill, 2003.
5. Ramachandran, Seetharaman. Digital VLSI systems design: a design manual for implementation of projects on FPGAs and ASICs using Verilog. Springer Science & Business Media, 2007.
6. Hassoun, Soha, and Tsutomu Sasao, eds. Logic synthesis and verification. Vol. 654.
SpringerScience & Business Media, 2001.
7. Grout, Ian. Digital systems design with FPGAs and CPLDs. Elsevier, 2011.

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College of Engineering, Pune

M. Tech. (Electronics-VLSI), Sem: I
VLSI Signal Processing

Teaching Scheme:	**Examination Scheme:**	**Credits Allotted:**
Theory: 04	End Semester Examination (Theory): 50 Marks	Credits: 04
	Internal Assessment (IA): 50 Marks	
	Total:100 Marks	Total Credits: 04

Course Pre-requisites:

The students should have knowledge of

1	Basic Electronics
2	Electronic Devices
3	Digital Signal Processing

Course Outcomes: After learning this course students will be able to

1	Use Iteration Bound for VLSI Signal Processing.
2	Apply Pipelining and Parallel processing for VLSI Signal Processing
3	Use Retiming for Signal Processing applications.
4	Apply Unfolding in VLSI Signal Processing.
5	Use Folding for Signal Processing

UNIT – I	**Iteration Bound**	**(09 Hours)**
	Introduction, Data-Flow Graph Representations, Loop Bound and Iteration Bound, Algorithms for Computing Iteration Bound: Longest Path Matrix and Minimum Cycle Mean algorithms - Iteration Bound of Multi-rate Data Flow Graphs.	
UNIT– II	**Pipelining and Parallel processing**	**(10 Hours)**
	Introduction, Pipelining for FIR Digital Filters: Cutset, Feed-forward Cutset, Data-Broadcast Structures, Fine-Grain Pipelining, Parallel Processing: Designing a Parallel FIR System, Pipelining for Low Power, Parallel Processing for Low Power	
UNIT – III	**Retiming**	**(10 Hours)**
	Introduction, Quantitative Description of Retiming, Properties of Retiming, Solving systems of Inequalities, Cutset Retiming and Pipelining, Retiming for Clock Period Minimization, Retiming for Register Minimization	
UNIT – IV	**Unfolding**	**(09 Hours)**
	Introduction, An Algorithm for Unfolding, Properties of Unfolding, CriticalPath, Unfolding, and Retiming, Applications of Unfolding: Sample Period Reduction and Parallel Processing	
UNIT – V	**Folding**	**(10 Hours)**

	Introduction, Folding Transformation, Register Minimization techniques: Lifetime Analysis, Data Allocation using Forward-Backward Register Allocation, Register Minimization in Folded Architectures: Biquad Filter and IIR Filter examples, Folding of Multi rate Systems	

Text Book/ Reference Books:
1. Parhi, Keshab K. VLSI digital signal processing systems: design and implementation. John Wiley & Sons, 2007.
2. Proakis, John G. Digital signal processing: principles, algorithms, and applications, 4/E. Pearson Education India, 2007.
3. Kalya, Shubhakar, Muralidhar Kulkarni, and K. S. Shivaprakasha, eds. Advances in Communication, Signal Processing, VLSI, and Embedded Systems: Select Proceedings of VSPICE 2019. Springer, 2020.
4. Mitra, Sanjit Kumar. Digital signal processing: a computer-based approach. Vol. 1221. New York, NY, USA:: McGraw-Hill, 2011.

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M. Tech. (Electronics-VLSI), Sem: I
SYSTEM ON CHIP

Teaching Scheme:	**Examination Scheme:**	**Credits Allotted:**
Theory: 04	End Semester Examination (Theory): 50 Marks	Credits: 04
	Internal Assessment (IA): 50 Marks	
	Total:100 Marks	Total Credits: 04

Course Pre-requisites:

The students should have knowledge of

1	Electronic Devices
2	Microprocessor and Microcontroller
3	Switching Theory and Logic Design

Course Objectives:

1	Design, optimization, and programming a modern system-on-chip
2	SoC design with on-chip memories and communication networks, I/O interfacing.
3	Signal integrity aware SoC design and scheduling algorithms.

Course Outcomes: After learning this course students will be able to

1	Examine the performance of SOC-based design using advanced techniques.
2	Apply timing analysis for a SoC-based design
3	Create interconnection structures in a SoC-based system design.
4	Analysis of IP-based System Design
5	SoC design, Implementation, and testing

UNIT – I	**Introduction to SoC**	**(09 Hours)**
	Introduction: Driving Forces for SoC, Components of SoC, Design flow of SoC, Hardware/Software nature of SoC, Design Trade-offs, SoC Applications	
UNIT– II	**System-level Design**	**(10 Hours)**
	Processor selection, Concepts in Processor Architecture: Instruction set architecture (ISA), elements in Instruction Handing-Robust processors: Vector processor, VLIW, Superscalar, CISC, RISC, Processor evolution: Soft and Firm processors, Custom-Designed processors, On-chip memory	
UNIT – III	**SoC Interconnection**	**(10 Hours)**
	SoC Interconnection Structures, Bus-based Structures, AMBA Bus. Network on Chip (NoC) Interconnection Structures, topologies, switching strategies, routing algorithms, flow control, Quality of Service, Reconfigurability in communication	

	architectures.	
UNIT – IV	**IP based system design**	**(09 Hours)**
	Introduction to IP Based design, Types of IP, IP across design hierarchy, IP life cycle, Creating and using IP, Technical concerns on IP reuse, IP integration, IP evaluation on FPGA prototypes.	
UNIT – V	**SOC implementation and SOC Testing**	**(10 Hours)**
	Study of processor IP, Memory IP, wrapper Design, Real-time operating system (RTOS), Peripheral interface and components, High-density FPGAs, EDA tools used for SOC design. Manufacturing test of SoC: Core layer, system layer, application layer,	

Text Book/ Reference Books:

1. Flynn, Michael J., and Wayne Luk. Computer system design: system-on-chip. John Wiley & Sons, 2011.
2. Al-Hashimi, Bashir M., ed. System-on-chip: next generation electronics, IET, 2006.
3. Ahmed Jerraya and Wayne Wolf, Multiprocessor Systems-on-Chips (Systems on Silicon Series), First Edition, Morgan Kaufmann, 2010.
4. Pasricha, Sudeep, and Nikil Dutt. On-chip communication architectures: system on chip interconnect. Morgan Kaufmann, 2010.
5. Flynn, D., Aitken, R., Gibbons, A., & Shi, K. Low power methodology manual: for system-on-chip design. Springer Science & Business Media, 2007.
6. Wang, Laung-Terng, Charles E. Stroud, and Nur A. Touba. System-on-chip test architectures: nanometer design for testability. Morgan Kaufmann, 2010.
7. Wayne Wolf, "Modern VLSI Design: IP Based Design", Prentice-Hall India, 2009.

Lab Practice – I

List of experiments:

1. Introduction to HDL and different types of modelling.
2. To model HDL code to describe the functionality of all the basic logic gate. Compile and simulate the code to obtain the timing waveform. Draw the RTL design using data flow of architectural modelling.
3. To model HDL code to describe the functionality of half adder, full adder, half subtractor, full subtractor. Compile and simulate the code to obtain the timing waveform. Draw the RTL design using data flow and structural modelling (as "Component Instantiation").
4. To model HDL code to describe the functionality of MUX, DEMUX, Encoder and Decoder. Compile and simulate the code to obtain the timing waveform. Draw the RTL design using data flow and structural modelling.
5. To model HDL code to describe the functionality of D-FF and D-Latch. Compile and simulate the code to obtain the timing waveform. Draw the RTL design using data flow and structural modelling.
6. Implement and verify all logic gates, Half adder, Full adder, Half subtractor and Full subtractor in FPGA Kit.
7. To model HDL code to describe the functionality of 4-bit parallel Adder using two full adders as "Component Instantiation". Compile and simulate the code to obtain the timing waveform and draw the RTL design.
8. To model Universal Shift register using HDL and Implement in FPFA Kit.
9. Project 1: Application based Hardware implementation.
10. Project 2: Application based Hardware implementation.

Software: VIVADO (Xilinx) tool

Hardware: FPGA Boards (NEXYS A7, GENESYS 2)

Lab Practice – II

List of experiments:

1. To model HDL code for up counter, down counter and up-down counter. Compile andsimulate the code to obtain the timing waveform. Draw the RTL design.
2. To model HDL code for sequence detector. Compile and simulate the code to obtain the timing waveform. Draw the RTL design.
3. To interface PMOD BT module with using FPGA kit
4. To interface PMOD GPS module with FPGA kit
5. To interface PMOD WIFI module with FPGA kit
6. To model HDL code for speed control of stepper motor and interface stepper motor with FPGA kit
7. To interface camera module with FPGA kit
8. To interface PMOD TEMP module with using FPGA kit
9. Project 1: Application based Hardware implementation.
10. Project 2: Application based Hardware implementation.

Software: VIVADO (Xilinx) tool

Hardware: FPGA Boards (NEXYS A7, GENESYS 2, KINTEX-7, PMOD BT, PMOD GPS, PMOD WIFI, Stepper motor, Camera module, PMOD TEMP)

M. Tech (Electronics-VLSI)(2023-24)

Semester II					**Total Duration: 24hrs/week** **Total Marks : 500** **Total Credits: 20**				
Subjects	**Teaching Scheme (Hrs) Hrs./Week**		**Examination Scheme (Marks)**						**Credits**
	L	**P**	**Theory**	**Internal Assessment**	**TW**	**PR**	**Oral**	**Total**	
Analog CMOS Design	04	--	50	50	--	--	--	100	04
VLSI Test and Testability	04	--	50	50	--	--	--	100	04
Low Power IC Design	04	--	50	50	--	--	--	100	04
Open Elective - II	04	--	50	50	--	--	--	100	04
Lab Practice - I	--	04	--	--	25	--	25	50	02
Lab Practice - II	--	04	--	--	25	--	25	50	02
Total	**16**	**8**	**200**	**200**	**50**	--	**50**	**500**	**20**

List of Open Electives

Open Elective - I	**Open Elective - II**
VLSI Signal Processing	Current Mode Circuit
System on Chip (SoC)	RF Circuit Design

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College of Engineering, Pune

M. Tech. (Electronics-VLSI), Sem: II
Analog CMOS Design

Teaching Scheme:	**Examination Scheme:**	**Credits Allotted:**
Theory: 04	End Semester Examination (Theory): 50 Marks	Credits: 04
	Internal Assessment (IA): 50 Marks	
	Total:100 Marks	Total Credits: 04

Course Pre-requisites:

The students should have knowledge of

1	Basic Electronics
2	Electronic Devices
3	VLSI Design

Course Outcomes: After learning this course students will be able to

1	Apply modeling for MOS circuits.
2	Design Analog CMOS sub-circuits.
3	Conceptualize CMOS amplifiers.
4	Characterize CMOS OP AMPs
5	Concepts of High-Performance CMOS OP AMPs

UNIT – I	**MOS Devices and Modeling**	**(09 Hours)**
	Introduction to Analog Design and its Tradeoffs, The MOS Transistor: Concept of Threshold Voltage, Derivation of I_D, Operation of MOSFET under various regions, Concept of g_m , MOS Capacitance, MOS Modeling : Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Sub-threshold MOS Model.	
UNIT– II	**Analog CMOS Sub-Circuits**	**(10 Hours)**
	Introduction to CMOS Sub-circuits, MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors, Current and Voltage References, Band gap Reference.	
UNIT – III	**CMOS Amplifiers**	**(10 Hours)**
	Introduction to CMOS Basic Amplifiers, Active pMOS load Inverters, Current Source Inverters, Push pull Inverters, Differential Amplifiers: Introduction, Design Process and Design example, Cascode Amplifiers: Introduction, Design Process and Design example	
UNIT – IV	**CMOS Operational Amplifiers**	**(10 Hours)**
	Review of Operational Amplifier concepts, Introduction to two stage OP AMP, OP AMP Design Process, Design of CMOS OP AMPs, Compensation of OP AMPs, Design of Two-Stage OP AMPs, Power-Supply Rejection Ratio of Two -Stage OP AMPs,	

	Cascode OP AMPs, Measurement Techniques of OP AMP	
UNIT – V	**Introduction to High Performance CMOS OP AMP**	**(09 Hours)**
	Introduction to High Performance CMOS OP AMP such as Buffered OP AMP, High Speed/Frequency OP AMP: Introduction Switched OP AMP, Current Feedback OP AMP , Parallel path OP AMP, Micro Power OP AMP: Introduction and Design Example, Low Noise OP AMP, Low Voltage OP AMP	

Text Book/ Reference Books:
1. Philip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Analysis and Design of Analog Integrated Circuits -Wiley India, Fifth Edition, 2010.
3. David A. Johns, Ken Martin, Analog Integrated Circuit Design, Wiley Student Edn, 2013.
4. Behzad Razavi, Design of Analog CMOS Integrated Circuits, TMH Edition, 2002.
5. Baker, Li and Boyce, CMOS: Circuit Design, Layout and Simulation, PHI, 2010.

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College of Engineering, Pune

M. Tech. (Electronics-VLSI), Sem: II
VLSI Test and Testability

Teaching Scheme:	**Examination Scheme:**	**Credits Allotted:**
Theory:04	End Semester Examination (Theory):50Marks	Credits:04
	Internal Assessment (IA): 50Marks	
	Total:100Marks	TotalCredits:04

Course Pre-requisites:

The students should have knowledge of

1	Basic Electronics
2	Digital Electronics

Course Objectives:

1	Introduction of different types of faults in digital circuits.
2	To introduce logic and fault simulation.
3	To introduce testability measures.
4	Study BIST techniques for improving testability
5	To Study boundary scan based test architectures and study of fault diagnosis.

Course Outcomes: After learning this course students will be able to

1	Recognize different fault models.
2	Understand different modeling circuits and algorithms for fault simulation
3	Identify different scan design methods.
4	Recognize the BIST techniques for improving testability
5	Understand the boundary scan based test architectures and system fault diagnosis.

UNIT– I	**Testing and Fault Modeling**	**(10Hours)**
	Role of Testing, Digital and Analog VLSI Testing, , Types of Testing, Modeling Digital Circuits at Logic Level, Register Level and Structural Models. Levels of Modeling. Fault models - Stuck-at faults, Bridging faults, intermittent faults	
UNIT–II	**Logic and Fault Simulation**	**(09Hours)**
	Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.	
UNIT– III	**Testability Measures**	**(10Hours)**
	SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.	

UNIT– IV	**Built-In Self-Test**	**(09Hours)**
	BIST Process, Pattern Generation, LFSR for pattern generation , Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-PerScan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.	
UNIT– V	**Boundary Scan and system level Diagnosis**	**(10Hours)**
	TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions. Concept of Redundancy, Spatial Redundancy, Time Redundancy, Error Correction Codes. Reconfiguration Techniques; Yield Modeling, Reliability and effective area utilization	

Text Books/Reference Books:

1. M. Bushnell, V. Agrawal, Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits, Kluwer Academic Publishers, 2004.
2. Z. Navabi, Digital System Test and Testable Design, Springer, 2011.
3. Miron Abramovici, Melvin A. Breur, Arthur D. Friedman, Digital Systems Testing and Testable Design, Jaico Publishing House, 2001.
4. M. Abramovici, M. A. Breuer and A.D Friedman, Digital Systems and Testable Design, Jaico Publishing House, 1990.
5. P.K. Lala, Digital Circuits Testing and Testability, Academic Press, 1997.
6. L. T. Wang, C. W. Wu, and X. Wen, VLSI Test Principles and Architectures, Morgan Kaufmann, 2006.
7. Robert J. Feugate, Jr., Steven M. Mentyn, Introduction to VLSI Testing, Prentice Hall, Englehood Cliffs, 1998.
8. Alfred Crouch, Design for Test for Digital ICs and Embedded core systems, Prentice Hall, 1999.

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M. Tech. (Electronics-VLSI), Sem: II
Low Power IC Design

Teaching Scheme:	**Examination Scheme:**	**Credits Allotted:**
Theory: 04	End Semester Examination (Theory): 50 Marks	Credits: 04
	Internal Assessment (IA): 50 Marks	
	Total:100 Marks	Total Credits: 04

Course Pre-requisites:

The students should have knowledge of

1	Basic Electronics
2	VLSI Design
3	Digital circuits

Course Outcomes: After learning this course students will be able to

1	To carry out research and development in the area of Low Power VLSI circuits.
2	Apply techniques to improve power consumption of VLSI circuits
3	Utilize logic simulation methods to design Low Power VLSI circuits.
4	Apply logic-level, architecture-level and system-level techniques in various designs to optimize power consumption of the VLSI circuits.
5	Implement practical and state of the art Low Power VLSI design, suitable for real life and Industry applications.

UNIT – I	**Introduction to Low Power VLSI design**	**(09 Hours)**
	Introduction to Low Power VLSI design, Importance of low power design, Challenges in low power VLSI design, Application of Low Power VLSI circuits, Power analysis of CMOS circuits, Themes of Low Power VLSI design, Supply voltage scaling, Reduction of load capacitances. Emerging Low power approaches.	
UNIT– II	**Device and Technology**	**(10 Hours)**
	Device and Technology impact on Low Power: Dynamic Dissipation in CMOS, Transistor Sizing and Gate Oxide Thickness, Impact of Technology Scaling, and Technology and Device Innovation Simulation Power analysis: SPICE circuit simulators, gate-level logic simulation, capacitive power estimation, static state power, gate-level capacitance estimation, architecture-level analysis, data correlation analysis in DSP systems, Monte Carlo simulation	
UNIT – III	**Probabilistic power analysis**	**(10 Hours)**
	Probabilistic power analysis: random logic signals, probability and frequency, probabilistic power analysis techniques, signal entropy Low Power Circuits: Transistor and Gate Sizing, Network	

	Restructuring, and Reorganization Special Flip Flops & Latches design, high capacitance nodes, low-power digital cell library Logic level: gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic.	
UNIT – IV	**Low-power architecture and systems**	**(10 Hours)**
	Low-power architecture and systems: power and performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low-power arithmetic components Low-power clock distribution: power dissipation in clock distribution, single driver vs. distributed buffers, zero skew vs. tolerable skew, chip and package co-design of clock network, Leakage currents in DSM technology Leakage reduction techniques: process level and circuit level Design time techniques	
UNIT – V	**Techniques for Power Reduction**	**(09 Hours)**
	Special Techniques: Power Reduction in Clock Networks, CMOS Floating Node, Low Power Bus Delay Balancing, and Low Power Techniques for SRAM, Variation-tolerant design Adiabetic logic circuits, battery-driven system design CAD tools for low power (software design for low power), case studies (low power static RAM architecture)	

Text Book/ Reference Books:

1. Gary K. Yeap, Practical low power digital VLSI design. Springer Science & Business Media, 2012.
2. Jan M. Rabaey and Pedram Massoud, eds. Low power design methodologies, Springer Science & Business Media, 2012.
3. Kaushik Roy and Sharat C. Prasad. Low-power CMOS VLSI circuit design. John Wiley & Sons, 2009.
4. Behzad Razavi, Design of Analog CMOS Integrated Circuits, TMH Edition, 2002.
5. Kiat-Seng Yeo, Samir S. Rofail, and Wang Ling Goh. CMOS/BiCMOS ULSI: low voltage, low power, (2002).
6. Wolfgang Nebel and Mermet eds. Low power design in deep submicron electronics, Springer Science & Business Media, 2013.

Bharati Vidyapeeth
(Deemed to be University)
College of Engineering, Pune

M. Tech. (Electronics-VLSI), Sem: II
Open Elective-II: Current Mode Circuit

Teaching Scheme:	**Examination Scheme:**	**Credits Allotted:**
Theory: 04	End Semester Examination (Theory): 50 Marks	Credits: 04
	Internal Assessment (IA): 50 Marks	
	Total:100 Marks	Total Credits: 04

Course Pre-requisites:

The students should have knowledge of

1	Switching Theory and Logic Design
2	Basic Electronic
3	CMOS Design

Course Outcomes: After learning this course students will be able to

1	Current mode circuits over voltage mode counterparts.
2	Understand Trans-linear principle for current mode circuits along with concept of Nullator and Norator
3	Understand the properties of different current mode analog building blocks
4	Apply current mode approach in Non-Linear Circuits
5	Apply current mode Integrated circuits

UNIT – I	**Introduction to Current Mode Circuits**	**(09 Hours)**
	Introduction, comparison of current mode circuits with voltage mode circuits; advantages, some current mode circuits: vector difference circuit, TL one quadrant squaring circuit, absolute value circuit, TL multiplier and divider	
UNIT– II	**Current Mode Circuit Principle**	**(10 Hours)**
	Current mode circuits: Principle of operation, trans-linear principle, concept of Nullator and Norator, Some BJT and MOS based current mode blocks: CCI, CCII, internal structures, principle of operation; port relationship, analysis and applications; multi-output current conveyors: Construction, advantages	
UNIT – III	**Current Mode Building Blocks**	**(10 Hours)**
	Current mode Building blocks: CCCII(+), CCCII(-), OTA, OTRA internal structures, principle of operation; port relationship, analysis and applications; multi-output current conveyors: Construction, advantages. use of transconductance amplifier as variable resistance, inductance simulator, oscillator and filter.	
UNIT – IV	**Non-linear applications**	**(10 Hours)**

	Non-linear applications: Schmitt trigger, multiplier; Operational Mirror Amplifier (OMA): principle of operation, applications as voltage controlled current source, current controlled current source, voltage-controlled voltage source, current controlled voltage source, high CMRR instrumentation amplifier	
UNIT – V	**Current mode Integrated circuit and applications**	**(09 Hours)**
	CFOA (Current feedback operational amplifier) AD844 IC, Port relationship, circuit analysis and its applications, OTA (CA3080) IC, Port relationship, circuit analysis and its applications, Current feedback amplifier with DC gain (LT1228) IC, Port relationship, circuit analysis and its applications.	

Text Book/ Reference Books:

1. David Haigh, F. J. Lidgey, Chris Toumazou, eds. Analogue IC design: the current-mode approach. Institution of Engineering and Technology, 1998.
2. Raj Senani, D. R. Bhaskar, A. K. Singh. Current conveyors: variants, applications and hardware implementations. Vol. 560. Switzerland: Springer International Publishing, 2015.
3. Raj Senani, D. R. Bhaskar, A. K. Singh, and V. K. Singh. Current feedback operational amplifiers and their applications. Springer New York, 2013.
4. P V Ananda Mohan, Current-mode VLSI analog filters: design and applications. Springer Science & Business Media, 2003.
5. Mohammed Ismail, Mohamad Sawan, Analog Circuits and Signal Processing, 2013.
6. Fei Yuan, CMOS current-mode circuits for data communications, Springer Science & Business Media, 2007.
7. Sajal K. Paul, IC Analog Filter Design, lambert academic publishing, 2011.

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M. Tech. (Electronics-VLSI), Sem: II
Open Elective-II: RF Circuit Design

Teaching Scheme:	**Examination Scheme:**	**Credits Allotted:**
Theory:04	End Semester Examination (Theory):50Marks	Credits:04
	Internal Assessment (IA): 50Marks	
	Total:100Marks	TotalCredits:04

Course Pre-requisites:

The students should have knowledge of

1	Analog IC design
2	Communication systems

Course Objectives:

1	Introduction to RF modulation.
2	Introduce the working of RF components.
3	To introduce mixers and oscillators.
4	Study of different RF amplifiers and synthesizer.
5	To Study LNA topologies.

Course Outcomes: After learning this course students will be able to

1	Understand the basic concepts of RF design and modulation
2	Understand the behavior of RF components
3	Understand the operation of mixers and oscillators.
4	Identify different RF amplifiers and synthesizers.
5	Comprehend the different LNA topologies & design techniques

UNIT– I	**Introduction to RF design**	**(10Hours)**
	Basic Concepts in RF Design, Analog and digital modulation of RF circuits, Comparison of various techniques for power efficiency, Coherent and non-coherent detection, Mobile RF communication and basics of Multiple Access techniques, Receiver and Transmitter architectures, Transmission media and Reflections, Maximum power transfer, Scattering Parameters	
UNIT–II	**RF Components**	**(09Hours)**
	RF Passive Components: Characteristics of passive IC components at RF frequencies – interconnects, resistors, capacitors, inductors and transformers – Transmission lines. RF active components: BJT and MOSFET behavior at RF frequencies, modeling of the transistors, Noise performance and limitations of devices, integrated parasitic elements at high frequencies and their monolithic implementation.	
UNIT– III	**Mixers and Oscillators**	**(10Hours)**

	Passive and Active Mixers: multiplier-based mixers, sub-sampling mixers, diode-ring mixers, Oscillators: Basic Principles, Cross-Coupled VCO, Phase Noise, Noise power and trade off. Resonator VCO designs, Quadrature and single sideband generators.	
UNIT– IV	**RF amplifiers and synthesizers**	**(09Hours)**
	RF power amplifiers – Class A, AB, B, C, D, E and F amplifiers, modulation of power 36 amplifiers, linearity considerations Radio frequency Synthesizers- PLLS, Various RF synthesizer architectures and frequency dividers, Design issues in integrated RF filters.	
UNIT– V	**Low Noise Amplifiers**	**(10Hours)**
	SNR, LNA topologies. MOS LNA, BJT LNA, noise cancelling LNA, Gm-boosting LNA, Noise Figure, LNA linearization, LNA Stability, power constrained noise optimization, linearity and large signal performance. Linearity consderations,1-dB compression, IIP, THD estimation	

Text Books/Reference Books:

1. T. H. Lee, Design of CMOS RF Integrated Circuits, Cambridge University Press, 2003.
2. B. Razavi, RF Microelectronics, Pearson, 2012.
3. R. Jacob Baker, H.W. Li, D.E. Boyce, CMOS Circuit Design, layout and Simulation, PHI, 2019.
4. Y. P. Tsividis, Mixed Analog and Digital Devices and Technology, TMH, 2002.
5. Bosco Leung, VLSI for Wireless Communication, Springer, 2011.

Lab Practice – I

List of experiments:

1. Design the second-generation current conveyor (CCII) block and verify the port relationship.
2. Design the third-generation current conveyor (CCIII) block and verify the port relationship.
3. Design the differential difference current conveyor transconductance amplifier (DDCCTA) block and differential voltage current conveyor transconductance amplifier (DVCCTA) and verify the port relationships.
4. Design and analyse a first-order universal filter based on CCII and verify the output response of the filter.
5. Design and analyse the oscillator based on CCII and verify the output response of the oscillator.
6. Design and analyse a first-order universal filter and oscillator based on IC AD844 (monolithic IC) and verify the output response of the circuits. Implement the hardware circuit and verify the simulation results.
7. Design and analyse a second filter and oscillator based on IC CA3080 (monolithic IC) and verify the output response of the circuits. Implement the hardware circuit and verify the simulation results.
8. Design and analyse the first and second universal filters and oscillators based on IC LT1228 (monolithic IC) and verify the output responses of the circuits. Implement the hardware circuit and verify the simulation results.
9. Project 1: Application-based Hardware Implementation
10. Project 2: Application-based Hardware Implementation

Software: Cadence OrCAD tool/cadence Virtuoso/ Synopsys/Mentor Graphics/ SPICE.

Hardware: IC AD844, IC CA3080, IC LT1228

Lab Practice – II

List of experiments:

1. Characteristics of MOS and MOS Modeling
2. Design of MOS diode.
3. Design of current mirrors.
4. Design of the basic current sink and sources
5. Design of pMOS load inverting amplifier and verify the output response of the amplifier.
6. Design push pull inverting amplifier and verify the output response of the amplifier.
7. Design differential amplifier and verify the output response of the amplifier.
8. Design a two-stage CMOS operational amplifier and analyze the different parameters.
9. Project 1: Application-based Circuit Implementation
10. Project 2: Application-based Circuit Implementation

Software: Cadence OrCAD tool/cadence Virtuoso/ Synopsys/Mentor Graphics/SPICE.

Semester III					**Total Duration: 08 hrs/week** **Total Marks : 250** **Total Credits: 20**				
Subjects	**Teaching Scheme (Hrs) Hrs./Week**		**Examination Scheme (Marks)**						**Credits**
	L	**P**	**Theory**	**Internal Assessment**	**TW**	**PR**	**Oral**	**Total**	
Seminar	--	02	--	--	50	--	50	100	05
Dissertation Stage - I	--	06	--	--	100	--	50	150	15
Total	**--**	**08**	**--**	**--**	**150**	**--**	**100**	**250**	**20**

Semester IV					**Total Duration: 08 hrs/week** **Total Marks: 250** **Total Credits: 20**				
Subjects	**Teaching Scheme (Hrs) Hrs./Week**		**Examination Scheme (Marks)**						**Credits**
	L	**P**	**Theory**	**Internal Assessment**	**TW**	**PR**	**Oral**	**Total**	
Dissertation Stage - II	--	08	--	--	150	--	100	250	20
Total	**--**	**08**	**--**	**--**	**150**	--	**100**	**250**	**20**