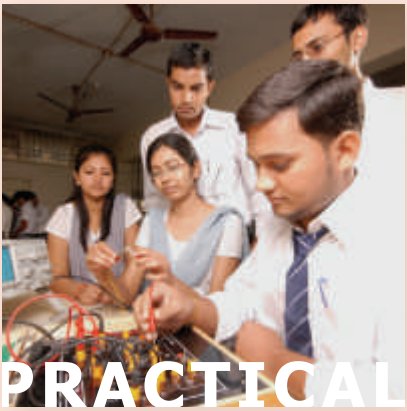
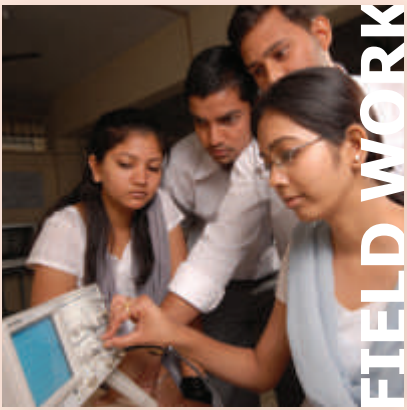
BHARATI VIDYAPEETH UNIVERSITY,
Pune.

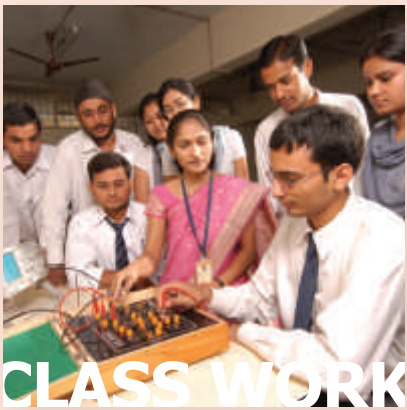
(Established under Section 3 of UGC ACT 1956)



COURSE STRUCTURE AND SYLLABUS

B. Tech. (E&TC)
(Sem. III & IV)





COURSE STRUCTURE & SYLLABUS

BHARATI VIDYAPEETH UNIVERSITY, PUNE

B. Tech. (E & TC) (Sem. III & IV)

HIGHLIGHTS

Bharati Vidyapeeth University College of Engineering (BVUCOE) is the largest Engineering College in Maharashtra with an intake of 700 students in each academic year. Imparting quality technical education from Under Graduate to Doctorate Level, BVUCOE is probably the only Engineering College in India with an accreditation from both NAAC as well as NBA. The faculty at BVUCOE boasts of highly qualified academicians, a quality that is further emphasized by the fact that 15 of them are presently pursuing their Ph.D. degree.

BVUCOE has been ranked 29th amongst the Top 50 Technical Schools of India in survey conducted by DATAQUEST-IDC. We have enjoyed a ranking in this list for the last 4 years. Research is of utmost importance in all our programs. A total of 113 research papers were published in the academic year 2007-2008.

Currently we have 12 ongoing research projects. The infrastructure of BVUCOE is state-of-the-art with 62 classrooms, 59 laboratories and a well-stocked library that currently holds 27,130 titles. The college has an international presence with MoUs signed with the North Carolina A&T State University (Greensboro, USA), University of Venice (Italy), Actel Corporation (USA).Corporate interaction is also inculcated in our programs through our association with Oracle India Ltd., Infosys Ltd. and Tata Consultancy Services.

SALIENT FEATURES

The world of today is ever dependent on a rapidly versatile and rapidly growing communications infrastructure. Convergence is the need of the hour where voice, data and video over single networks are likely to be offered with a very high quality of service. The consumer market for broadband services, VOIP and Internet TV is increasing at a fast pace.

The near future will see IP Multimedia sub systems (IMS) as a bedrock of the Next Generation Networks (NGNs).

To cope with this highly specialised sphere of technology, the course has been designed with all key relevant inputs being provided. Our aim is to develop innovative engineering skills which are essential in meeting the critical demands of the fast and furiously advancing electronics and telecommunications industry.

MAJOR EQUIPMENT

Mixed Signal Oscilloscope, Vector Voltmeter, Digital Storage Oscilloscope, Wobbuloscope, Powerscope, Allen-Bradley PLC with RSLogix500 software, Ratio Control Unit Trainer, ICAP 4, DSP Processor Training Boards

SOFTWARE

ORCAD, XLINX 3.1, Altera, MATLAB, LabView, ALDEC, Code Composer Studio, Libero

LABORATORIES

ACTEL-VLSI Lab, Microelectronics Laboratory, Digital Electronics Laboratory, Network and Lines Laboratory, Electric Circuit Design and Project Laboratory, Communication Laboratory, Microprocessor and Microcontroller Laboratory, Computer Networking Laboratory, DSP and Image Processing Laboratory, Electronic Instrumentation and

Measurements, Power Electronics Laboratory, Instrumentation and Control Laboratory, Biomedical Laboratory, Computer Lab

STRUCTURE & EXAMINATION PATTERN

B. Tech. - E & TC

Semester III

Total Duration : 28Hrs/Week
Total Marks : 750

Subject Code	Subject	Teaching Scheme		Examination Scheme				Total
		L	P	Theory	Unit Test	TW & Pr	TW & Or	
K50221	Electronic Devices	04	02	80	20	50	50	200
K50222	Network Analysis	04	02	80	20	50	-	150
K50223	Fundamentals of Instrumentation & Control	04	02	80	20	-	50	150
K50224	Data Structures & Files	04	02	80	20	-	50	150
K70201	Engineering Mathematics - III	04	-	80	20	-	-	100
	Total	**20**	**08**	**400**	**100**	**100**	**150**	**750**

Teaching Scheme		Examination Scheme				Total
Lectures	Practical	Theory	Unit Test	T. W. & Pr	T. W. & Or.	
20	08	400	100	100	150	750

Semester IV

Total Duration : 28Hrs/Week
Total Marks : 750

Subject Code	Subject	Teaching Scheme		Examination Scheme				Total
		L	P	Theory	Unit Test	TW & Pr	TW & Or	
K50227	Electronic Circuits	04	02	80	20	50	50	200
K50228	Analog Communication	04	02	80	20	50	-	150
K50229	Digital Electronics	04	02	80	20	50	-	150
K50230	Computer Organization & Operating Systems	04	-	80	20	-	-	100
K50231	Signals & Systems	04	02	80	20	-	50	150
	Total	**20**	**08**	**400**	**100**	**150**	**100**	**750**

Teaching Scheme		Examination Scheme				Total
Lectures	Practical	Theory	Unit Test	T. W. & Pr.	T. W. & Or.	
20	08	400	100	150	100	750

RULES FOR CONDUCTING TESTS

Mode of the test

In each semester for each subject three tests shall be conducted. The schedule for the same will be declared at the commencement of academic year in the academic calendar.

Each test shall carry 20 marks.

University examination pattern has given weightage of 20 marks for the tests.

To calculate these marks following procedure is followed:

i) Out of the three tests conducted during the semester, the marks of only two tests in which the candidate has shown his/her best performance shall be considered, to decide the provisional marks in each subject.

ii) Average marks obtained in two tests in which students have performed well, shall be considered as provisional marks obtained by the student in the tests.

iii) If the candidate appears only for two tests conducted during the semester, he/ she will not be given benefit of the best performance in the tests.

iv) If the candidate appears only for one test conducted during the semester, to calculate the marks obtained in the tests it will be considered that the candidate has got 0 (zero) marks in other tests.

v) The provisional marks obtained by the candidate in class tests should reflect as proportional to theory marks. In cases of disparity of more than 15% it will be scaled down accordingly; These marks will be final marks obtained by the student. No scaling up is permitted.

vi) If the candidate is absent for theory examination or fails in theory examination his final marks for tests of that subject will not be declared. After the candidate clears the theory, the provisional marks will be finalized as above.

Paper Pattern for Tests

i) All questions will be compulsory with weightage as following

Question 1	-	7 marks
Question 2	-	7 marks
Question 3	-	6 Marks

ii) There will not be any sub-questions.

For granting the term it is mandatory to appear for all the three tests conducted in each semester.

Roll numbers allotted to the students shall be the examination numbers for the tests.

SEMESTER - III

K50221: ELECTRONIC DEVICES

TEACHING SCHEME		EXAMINATION SCHEME	
Lectures	: 04 Hrs/Week	Theory	: 80 Marks
Practical	: 02 Hrs/Week	Duration	: 03 Hours
		Unit Test	: 20 Marks
		T. W. & Pr.	: 50 Marks
		T. W. & Or.	: 50 Marks

Unit-I (08 Hours)

Semiconductor Materials & Passive Components:

Classification of materials on the basis of electrical conductivity, Intrinsic and extrinsic semiconductors, Conduction mechanism in extrinsic semiconductors, Carrier concentrations, Drift and diffusion mechanism, Drift and diffusion current densities, Semiconductor materials used in Optoelectronic devices, modern semiconductor devices and Integrated circuits- GaAs, SiGe, GaAsP. Study of resistor, inductor, capacitor, relay, switches, LED, photo-electric devices.

Unit-II (09 Hours)

Semiconductor Diodes and Applications:

A brief overview of following types of diodes, their peculiarities and applications Rectifier, Switching, Power, Tunnel, Shockley, Gunn, PIN.

Semiconductor P-N junction diode –Open circuited step graded junction, Metallurgical junction and ohmic contacts, Depletion region, Barrier potential, Forward and reverse biased diode operation. V-I characteristics equation of diode (no operation). Volt equivalent of temperature. Temperature dependence of V-I characteristics, DC load line, Forward and reverse dynamic resistance, Small signal and large signal diode models. Diode data sheet specifications- PIV, etc. switching diodes – Diode switching times, junction capacitance, (No derivation).

Voltage multiplier circuits: Working and comparison of voltage doubler, tripler and voltage quadrpler configurations. Limitations of voltage multiplier circuits. Clipping and clamping circuits: Series and parallel forms of clipping circuits, Biased clipper, their operation and transfer characteristics. Clamping circuits.

Unit-III (09 Hours)

BJT Biasing and Basic Amplifier Configurations:

An overview of different types of BJTs – Small signal and large signal low frequency types, switching/RF, Hetero-junction types. Peculiarities of these types and their application areas.

Need for biasing BJT, DC analysis of BJT circuits, typical junction voltages for cutoff, active and saturation regions. Voltage divider bias and its analysis for stability factors, Small signal- low frequency h-parameter model, Variation of h-parameters with operating point, Derivations for CE configuration for A, Rin, Ro, in terms of h-parameters, Comparison of performance parameters with CB and CC configurations in tabular form. Need for multistage amplifiers and suitability of CE, CC and CB configurations in multistage amplifiers. Small signal and DC data sheet specifications for BJT.

Unit-IV (08 Hours)

Field Effect Transistors:

An overview of different types of FETs viz. JFET, MOSFET, MESFET. Peculiarities of these types and their application areas.

JFET: JFET construction, symbol, basic operation, V-I characteristics, transfer characteristics (Shockley's equation), cut-off & pinch-off voltages, Trans-conductance, Input resistance & Capacitance. Drain to source resistance. Universal JFET bias curve. Biasing arrangements for JFET – Biasing against device variation, biasing for zero current drift. J F E T as voltage controlled current source. JFET data sheet specification – IDSS. Vp, gm, rd, RDS.

JFET Amplifiers: CS, CD, CG amplifiers. Analysis using small signal J F E T model.

Unit-V (08 Hours)

MOSFETs:

An overview of following MOSFET types –D- MOSFET, E-MOSFET, Power MOSFET. n-MOS, p-MOS and CMOS devices. Handling precautions for CMOS devices. D and E-MOSFET characteristics & parameters, non ideal voltage current characteristics viz. finite output resistance, body effect, sub threshold conduction, breakdown effects and

temperature effects. MOSFET Biasing, Introduction to MOFET as VLSI device.

Unit-VI (07 Hours)

Performance of BJT & FET Amplifiers & PCB Design:

Concept of frequency response, Human ear response to audio frequencies, significance of Octaves and Decades. The decibel unit. Square wave testing of amplifiers. Miller's theorem. Effect of coupling, bypass, junction and stray capacitances on frequency response for BJT and FET amplifiers.

Types of PCB, PCB design rules, Layout design, Artwork design, Fabrication process of single sided PCB. Different copper clad laminates, composition of solder metal.

List of Practicals

Study of Components (Resistor, Inductor, Capacitor, Relay, Switches, Transfer)

Study of CRO and Different modes of operation.

Study of simulation software for circuits.

Study of diode characteristics.

Study of BJT and FET characteristics.

Study of biasing BJT CE amplifier.

Study of biasing of FET CS and CD amplifier.

Frequency response of single stage BJT amplifier.

Square wave testing of BJT amplifier.

Design, build and Test small electronic circuit on PCB

Text Books/References

Thomas L. Floyd, "Electronic Devices", Pearson Education (sixth edition)

Millman Halkias, "Electronic Devices and Circuits", Tata McGraw Hill (20th reprint)

Millman Halkias, "Integrated Electronics", Tata McGraw Hill (20th reprint)

Syllabus for Un it Test:

Unit Test 1	Unit I & II
Unit Test 2	Unit III & IV
Unit Test 3	Unit V & VI

K50222: NETWORK ANALYSIS

TEACHING SCHEME		EXAMINATION SCHEME	
Lectures	: 04 Hrs/Week	Theory	: 80 Marks
Practical	: 02 Hrs/Week	Duration	: 03 Hours
		Unit Test	: 20 Marks
		T. W. & Pr.	: 50 Marks

Unit –I (09 Hours)

Simplification & Analysis Techniques(AC & DC circuits):

Sinusoidal seady state, Phases & phasor diagram. Energy Sources. Mesh and nodal analysis. Source transformation of impaction. N network theorems.

i) Superposition theorem
ii) Thevinin Theorem
iii) Norton Theorem
iv) Maximum power transfer theorem

Unit-II (07 Hours)

Resonance & its Applications:

Definition of figure of merits', Series resonance: current Bandwidth, impedance & Selectivity in series resonance. Parallel (anti) resonance: Application of resonance circuits including impedance transformation.

Unit-III (07 Hours)

Transient Response:

Initial Conditions in elements. A procedure for evaluating initial conditions. Solution of RC, RL, RLC step response using classical method. Solution of RC, RL and RLC step response using Laplace transform.

Unit-IV (09 Hours)

Four Terminal Networks:

Classification of four terminal networks (Symmetrical, Asymmetrical, Balanced & Unbalanced), Characteristic Impedance & propagation constant for symmetrical networks. Image &Iterative impedance for symmetrical networks.

Filter Fundamentals: Constant K type Low pass filter. Constant K type high pass filter. Constant K type Pass filter. Constant K type band pass filter. Constant K type band pass filter. Constant K type band stop filter. M-derived T and n sections of low pass filter. Composite Low pass filter.

Attenuators: Introduction. Nippers & decibels. Symmetrical T& n type attenuators.

Unit-V (08 Hours)

Network Functions:

Terminal pairs and ports. Network functions for one and two port networks. Poles & zeroes of network function. Time domain behaviour from pole zero plot.

Unit-VI (08 Hours)

Two port network parameters:

Introduction. Open circuit Impedance parameters. Short circuit . Admittance parameters.Hybrid parameters. Transmission parameters. Interrelation between different parameters. Inter connection of two port networks.

List of Practicals

To verify Thevnin's Theorem.

To verify Maximum power transfer Theorem.(ac and dc)

To plot frequency response of frequency selective network (Twin T or Wein Bridge).

To build & test series and parallel Resonance circuits (Fr, BW, Q calculations).

To design constant k BPF and LPF circuits , to plot frequency response & to find cut –off frequency.

To design constant BPF and BSF circuits, to plot frequency response & to find cut- off frequency.

Select any two port network & find Z-Y parameters.

To plot Poles & zeroes for one port driving poles function.

Measurement of Zo and gamma for T and pi network.

Design , build & test symmetrical T & pi attenuators (plot of attenuation versus load

resistance)

Text Books/References

D.Roy Choudhary, "Network & System", Wiley Eastern (2nd Edition)

M.E. Van Valkenburg, "Network Analysis", PHI (3rd Edition)

F.F.Kuo, "Network Analysis & Synthesis", John Wiley & Sons (2nd Edition)

Hayt & Kimmerly, "Engineering Circuit Analysis", McGraw- Hill International (2nd Edition)

Syllabus for Unit Test

Unit Test 1	Unit I & II
Unit Test 2	Unit III & IV
Unit Test 3	Unit V & VI

K50223: FUNDAMENTALS OF INSTRUMENTATION & CONTROL

TEACHING SCHEME		EXAMINATION SCHEME	
Lectures	: 04 Hrs/Week	Theory	: 80 Marks
Practical	: 02 Hrs/Week	Duration	: 03 Hours
		Unit Test	: 20 Marks
		T. W. & Or.	: 50 Marks

Unit -I (09 Hours)

Linear & Non-Linear Control System:

Introduction to linear & nonlinear control system , Elements of control systems, Open loop & closed loop , feedback & feed forward control systems. (Each control systems will be highlighted with real time applications).

Transfer function using block diagram reduction technique & signal flow graph using Mason's gain formula.

Unit –II (07 Hours)

Transient Response:

Time domain Analysis of linear control systems. First order & second order system. Error constant, steady state error, transient response specification.

Stability of control system , Routh – Hurwitz criterion and Root locus technique.

Unit-III (08 Hours)

Frequency Domain Analysis:

Frequency domain analysis ,frequency domain specification,Bode Plot-Gain margin and Phase margin, Mapping theorem and Nyquist Plot.

Unit-IV (09 Hours)

Transducers:

Characteristics , types of transducers for temperature (RTD, Thermocouple, Thermistor), Capacitance type level transducer , electromagnetic type flowmeter, pressure transducer, LVDT,Strain guage, Piezoelectric type accelerometer, photoelectric tachometer (Pick up)

Unit-V (08 Hours)

Signal Conditioning:

Signal conditioning circuits, for above transducers, study of synchros.

Unit-VI (07 Hours)

Instrumentation Control Devices:

Control actions: On/Off, P , PI , PD, PID,PLC: Architecture, comparison with relay logic.

Ladder Diagrams for simple applications.

List of Practicals

Study of Temperature Transducers.

Study of LVDT for displacement measurement.

Flow control using PID action.

Verification of ladder diagram using PLC.

Unit step and ramp response of the transfer function system using MATLAB.

To draw Root locus and Bode Plot using MATLAB.

Phasor plot of synchro system (Transmitter-Receiver).

Magnitude and phasor plot of lead network.

Magnitude and phasor plot of lag network.

Transient response of second order system.

Text Books/References

Nagrath and Gopal, "Control Systems"

A. K. Sawhney, "Electrical & Electronic Measurements & Instrumentation", Dhanpat Rai Co & Ltd.

C. D. Johnson, "Process Control Instrmentation Technology"

K.Ogata, "Modern Control Engg.", PHI

Syllabus for Unit Test

Unit Test 1	Unit I & II
Unit Test 2	Unit III & IV
Unit Test 3	Unit V & VI

K50224: DATA STRUCTURES & FILES

TEACHING SCHEME		EXAMINATION SCHEME	
Lectures	: 04Hrs/week	Theory	: 80 Marks
Practical	: 02Hrs/week	Duration	: 03 Hours
		Unit Test	: 20 Marks
		T. W. & Or.	: 50 Marks

Unit -I (08 Hours)

Review of 'C':

Array, Pointer, array and pointer,

Function: Parameter passing, Call by value by reference, scope rules, concept of recursion and recursive functions, functions and pointer, Structure and Union: Passing and returning structure and union as parameter of function structure/union and pointer. Input/output files: Concept, files operations

Types: sequential & random access files.

Unit –II (09 Hours)

Introduction to Data Structures:

Overview-alorithm, data structure, how to create a program, how to analyze the program. Abstract Data Type. Concept of sequential organization, concept of linear and non linear data structure, arrays ADT, storage representations (row major and column major) Concept of ordered list & polynomial representation using array. Searching and sorting technique: Searching: Basic search technique, sequential searching, binary search, indexed sequential search. Analysis of theses algorithms.

Unit-III (07 Hours)

Linear Data Structure using Linked Organization:

Concept of link organization. Singly linked list, doubly linked list, Circular linked list. Insertion, deletion & traversal on above data structures, Representation & manipulation of polynomial using linked list.

Generalized lists: Representation of polynomial using generalized list.

Unit-IV (09 Hours)

Stacks & Queues:

Stack: definition & examples, representing stack in C, implementing stack using linked list.

Example: infix, postfix and prefix(basic definition and examples, evaluating postfix expression, converting infix to postfix expression, program to convert infix to postfix).

Queues: The queue and its sequential representation, linked implementation of queues, circular queue, concept of priority queue.

Unit-V (08 Hours)

Trees:

Basic terminology, binary trees, binary tree representation, binary tree traversal, primitive operation on binary tree, Binary search trees-primitive operation binary search trees, Threaded binary trees, Traversak of threaded binary tree.

Unit-VI (07 Hours)

Graphs:

Concepts and terminology, Representation of graphs using adjacency matrix, adjacency matrix, adjacency list. Traversal; Depth first search, breadth first search. Algorithms for minimal spaning tree and shortest path.

List of Practical

(a) program to create & manipulate database using structure.
(b) program to add two polynomial using array of structure.

Program to implement primitive operation on Sequential file.

(a) Program to search for record from a given list of records stored in array using
   i) Linear search
   ii) Binary search

(b) Program to create Hash table & handle collision using linear probing without replacement.

Program to sort an array of names using

   i) Bubble sort

ii) Insertion sort
iii) Quick sort

(a) Program to implement following operation on singly linked list:

i) Create
ii) Delete
iii) Insert
iv) Display
v) Search

(b) Program to add two polynomials using linked list.

(a) program to implement stack using:

i) Array
ii) Linked list

(b) Program to convert an infix expression to postfix expression & evaluate the resultant expression.

Program to Implement Queue using: (i) Array (ii)linked list

Program to create a Binary search tree & Perform following primitive operation on it:

i) Search
ii) Delete
iii) Traversals(inorder, pre-order, post-order -recursive)
iv) Non-recursive in order traversal

Program to create a graph using adjacency list & traverse it using BFS & DPS methods

Text Books/Reference s

Yedidyah langsam, Moshe J Augenstein, Aaron M Tenenbaum, "Data structures using C and C++"; PHI (2nd edition)

Ellis Horowitz, SatarajSahni, "Fundamentals of Data Structures" Galgetia Books source

Brain W Kernighan and Denis M Ritchie, "The programming language", PHI (2nd edition)

Robert L Kruse, "Data structure & program design", PHI(3rd edition)

Syllabus for Unit Test

Unit Test 1	Unit I & II
Unit Test 2	Unit III & IV
Unit Test 3	Unit V & VI

K70201: ENGINEERING MATHEMATICS –III

TEACHING SCHEME
Lectures : 04Hrs/week

EXAMINATION SCHEME
Theory : 80 Marks
Duration : 03 Hours
Unit Test : 20 Marks

Unit -I (09 Hours)

Differential Equations:

Solution of linear differential equation of nth order with constant coefficients, Methods of variation of parameters, Cauchy's and legendry linear equation , Simultaneous linear differential equation, Total differential equations , Symmetrical simultaneous differential equations, Application to electrical circuits.

Unit –II (08 Hours)

Complex variables:

Functions of complex variables , Analytic function, Cauchy - Riemann equations, Conformal mapping, Bilinear transformation, Residue theorem, Cauchy's integral theorem and formulae.

Unit-III (09 Hours)

Transforms:

Fourier transform: Fourier integral theorem, Fourier sine and cosine integral, Fourier transform , Fourier sine and cosine transform,Inverse fourier transform, Discret fourier transform and its application.

Z-Transform: Defination, Properties, Inverse Z-Transform, Application to difference equatin, Realtionship between Z-Transform and Fourier transform.

Unit-IV (09 Hours)

Laplace transform:

Definition, Properties and theorem, Inverse laplace transform, method of finding inverse laplace transform, Laplace transform of unit step function, Dirac-delta functions, Periodic functions, Ramp functions, Error functions, First order bessel's function, Si(t),Ci(t),Ei(t). Applications to solution of linear differential equations.

Unit-V (09 Hours)

Vector Differentiation:

Vector Differentiation, Gradient, Divergence and curl, Directional derivative, Vector identies, Irrotational and solenoidal vectors fields.

Unit-VI (08 Hours)

Vector integration:

Line integral, Surface integral and volume integral, Work done, Gauss- divergence theorem, Stoke's theorem and Green's lemma, Application to electro magnetic field.

Text Books/References

Peter V. O' Neil, "Advanced Engineering Mathematics", 5e, Thomson Learning

Erwin Kreyszig, "Advanced Engineering Mathematics" Wiley Eastern Ltd.

Wylie C. R. and Barret L. C., "Advanced Engineering Mathematics", McGraw-Hill

M .D. Green Berg, "Advanced engineering mathematics", 2e, Pearson Education

B. S. Grewal, "Higher Engineering Mathematics" , Khanna publication, Delhi

P. N. and J. N. Wartikar, "Applied Mathematics, Volume I and II", Pune Vidyarthi Griha Prakhasan

Murray R. Spiegel, "Laplace Transform", Schaum's Outline Series International Edition

Syllabus for Unit Test

Unit Test 1	Unit I & II
Unit Test 2	Unit III & IV
Unit Test 3	Unit V & VI

SEMESTER - IV

K50227: ELECTRONIC CIRCUITS

TEACHING SCHEME		EXAMINATION SCHEME	
Lectures	: 04 Hrs/Week	Theory	: 80 Marks
Practical	: 02 Hrs/Week	Duration	: 03 Hours
		Unit Test	: 20 Marks
		T. W. & Or.	: 50 Marks
		T. W. & Pr.	: 50 Marks

Unit -I (09 Hours)

MOSFET Applications:

MOSFET: V-I characteristic equation in terms of W/L ratio, MOSFET scaling and small geometry effect, MOSFET capacitances. Modeling MOS transistor using SPICE. CMOS inverter, Static characteristic –Noise margin, threshold voltage, Layout and latch-up prevention, other logic gates-NAND and NOR gates.

POWER MOSFET: Construction-Lateral double diffused MOSFET, VMOSFET. Drive requirements, Comparison with power BJT. One example of drive for circuit for POWER

MOSFET.

POWER BJT: Power BJT construction, Data sheet specifications, Thermal resistance, Second Breakdown, Safe operating area (SOA), Thermal runway, BJT as a switch in display and relay drive applications, Drive considerations, Anti saturation circuits, Comparison with Power MOSFET.

Unit –II (07 Hours)

Large Signal AF BJT Amplifiers:

Block schematic of AF amplifiers. Classes of power amplifier – Class A , Class B , Class AB. An overview and applications of Class C and Class D amplifiers. Class A with resistive load. Transformer coupled class A amplifier, Class B Push – pull, Class AB, Complementary symmetry and Quasi – complementary. Efficiency analysis for Class A transformer coupled amplifier, Class B push – pull amplifier. Comparison of efficiencies of other configurations. Distortion in amplifiers, concept of Total Harmonic Distortion (THD).

Unit-III (08 Hours)

High Frequency, Small Signal BJT Amplifiers:

Behavior of transistor at high frequencies. Modified T equivalent circuit. High frequency hybrid n CE amplifier model. CE short circuit current gain zfor T and hybrid n models. Definitions and derivations for fa, f and fr . Amplifier bandwidth taking into account source and load resistances. Techniques to improve bandwidth. Single tuned, Double tuned and stagger tuned amplifiers. Unloaded and loaded Q. Effect of staggering on bandwidth (no derivations).

Unit-IV (08 Hours)

Feedback Amplifiers And Oscillators:

Concept of feedback . Negative and positive feedback. Classifications of amplifier based on feedback topology. (Voltage, Current, Transconductance and Transresistance amplifiers). Transfer gain with feedback. Advantages and disadvantage of negative feedback. Effect of feedback on input and output impedances and bandwidth of amplifier. Analysis of one circuit for each feedback topology.

Unit-V (07 Hours)

Oscillators :

Oscillator start mechanism, need of amplitude limiting. Study of following oscillator circuits(using BJT & FET) – (Derivations not expected) RC oscillators, phase shift and Wien bridge oscillator LC oscillator – General form of LC Oscillators. Hartley oscillator, Colpitts oscillator, Clapp oscillator, Crystal oscillator.

Unit-VI (09 Hours)

Linear Voltage Regulators And Voltage References:

Block schematic of linear regulators, Emitter follower regulator, Transistor series regulator and its analysis for performance parameters. 3 terminal floating, dual and adjustable regulator. Method of boosting output current using external series pass transistor. Performance parameters – Load and Line regulations, Ripple rejection, Output resistance and efficiency. Protection circuits – Reverse polarity protection,

over circuit, fold back current limiting, over voltage protection. Important data sheet specifications of linear regulators. Voltage references, their peculiarities and applications.

List of Practicals

Centre tapped bridge rectifier
Study of multistage amplifier
RC Oscillators(phase shift and wien bridge)
Class A transformer coupled, Class B push – pull amplifier – Efficiency calculations
Transistor inverter in relay and LED driving application
Tuned amplifiers – single and doubled tuned amplifiers
Voltage series, current series feedback amplifier
Voltage shunt and current shunt feedback amplifiers
Simulation of LC oscillators
Linear voltage regulators – Floating, Adjustable three terminal regulators, current boosting, CV and CC modes of operation

Text Books/References

Thomas L. Floyd, "Electronics devices", Pearson Educations (Sixth edition)
Donald A. Neamen, "Electronic circuit analysis & Design", Tata McGraw Hill (Second Edition)
Mark N. Horenstein, "Microelectronics Circuits and Devices", Prentice Hall (Second Edition)
Millman Halkias, "Electronics Devices and Circuits", Tata McGraw Hill
Millman Halkias, "Integrated Electronics", Tata McGraw Hill

Syllabus for Unit Test

Unit Test 1	Unit I & II
Unit Test 2	Unit III & IV
Unit Test 3	Unit V & VI

K50228: ANALOG COMMUNICATIONS

TEACHING SCHEME		EXAMINATION SCHEME	
Lectures	: 04Hrs/week	Theory	: 80 Marks
Practical	: 02Hrs/week	Duration	: 03 Hours
		Unit Test	: 20 Marks
		T. W. & Pr.	: 50 Marks

Unit -I (08 Hours)

Introduction To Communication:

Block Schematic of communication system, Base Band Singnals and their bandwidth requirement, RF Bands, Types of communication channels(Transmission Lines, Parallel wires, co-axial Cables, Waveguides and Optical Fiber).Necessity of Modulation.

Unit –II (08 Hours)

Amplitude Modulation:

Mathematical treatment and expression for AM, Frequency Spectrum, Modulation Index, Power Relation as applied to Sinusoidal Signal, Representation of AM wave, Mathematical treatment as applied to general signals in communication, Generation of AM using non-linear property.

Type of AM Transmitters: DSB-FC, DSB-SC, SSB, ISB &VSB, their Generation methods and Comparison in terms of bandwidth and Transmission Power requirement & Complexity(Block diagram treatment only)

Unit-III (09 Hours)

Angle Modulation:

Mathematical analysis of FM and AM using Sinusoidal Signals, Frequncy Spectrum, Mathematical treatment as applied to general Non-sinosoidal Signals, Modulation Index, Bandwidth requirement(all three relation), Narrowband and Wideband FM, Comparison of PM & FM, Direct and direct methods methods of FM generation, Need for Preemphasis, Comparison of AM and FM, Block diagram of PAM, PWM, PPM. Multiplexing technique-TDM, FDM

Unit-IV (07 Hours)

Noise:

Sources of Noise, Types of Noise, SNR, Noise Figure, Noise Temperature, Friss formula for Noise Figure, Noise Banwidth, Performance of AM(DSB, SSB & VSB) And FM in presence of Noise: Mathematical treatment.

Unit-V (09 Hours)

AM & FM Receiver:

Block diagram of AM and FM Receiver, Super heterodyne Receiver, Performance characteristic: Sensitivity, selectivity, Fidelity, Image Frequency Rejection, IFRR. Tracking, De-emphasis,Mixers.

AM Detectioin: Envelope detection, Syncronous detection, Practical diode detection, AGC, SSB and DSB detection methods.

FM Detection: Phase discriminator and Ratio Detector, Mathematical analysis of FM Detection.

Unit-VI (07 Hours)

Radiation and Propagation:

Concept of Radiation, Basic Antenna System(Dipole), Antenna parameters, Yagi-Antenna, Mechanism of Propagation: Ground Wave, Sky Wave, Space Wave, Duct,Tropospheric Scatter and Extraterrestrial Propagation, Concept of Fading and diversity reception.

List of Practicals

Study of AM Generation(DSB-FC)

Study of AM transmitter using Spectrum Analyzer.

Study of Envelope Detector-Practical diode detector.

Study of FM Generation.

Study of transmitter using Spectrum analyzer.

Study of FM detection- Ratio detector.

Measurement of Reseiver characteristics: Sensitivity, Selevctivity,Fidelity

Study of DSB-SC & SSB Generator using Spectrum Analyser.

Study of DSB-SC & SSB Detector

Measurement of antenna radiation pattern for different antenna

Text Books/References

B.P.Lathi, "Modern Digital and Analog Communication System", Oxford Press Publication

Kennedy & Devis, "Electronic Communication Systems", PHI

Dennis Roddy & Coolen, "Electronic Communication", PHI

Syllabus for Unit Test

Unit Test 1	Unit I & II
Unit Test 2	Unit III & IV
Unit Test 3	Unit V & VI

K50229: DIGITAL ELECTRONICS

TEACHING SCHEME		EXAMINATION SCHEME	
Lectures	: 04 Hrs/Week	Theory	: 80 Marks
Practical	: 02 Hrs/week	Duration	: 03 Hours
		Unit Test	: 20 Marks
		T. W. & Pr.	: 50 Marks

Unit -I (08 Hours)

Logic Families:

Parameter definitions -noise margin, power dissipation, voltage and current parameters, propagation delay. Typical values for TTL ,CMOS & ECL. Input / output profile for TTL & CMOS. TTL logic families-standard, Totem – pole, open collector, tri-state (concept & application). Significance of TTL sub families (L, H, LS, S) & MOS family-importance of (C,HC), PMOS, NMOS (inverter only) ,CMOS (inverter, AND & NOR). TTL-CMGS/CMOS-TTL interfacing, comparison of TTL & CMOS. TTL compatible high speed CMOS series.

Unit –II (08 Hours)

Binary Number Systems & Coding:

Binary number system: Signed number representation (1's, 2's complement & sign magnitude representation). Codes- BCD, GRAY, Seven Segment, ASCII code.

Principles of combinational logic: Canonicals forms don't care conditions, minimization techniques (K-maps up to 4 variables only). Quine-McCluskey method (4 variables). Design examples- code converters (binary to gray and gray to binary, BCD to 7 segment,
IC 7447,7448).

Unit-III (09 Hours)

Combinational Logic Circuits:

Digital comparators (2 - bit, 4- bit using IC 7485), parity generation and checking (1 C 741'80). Design methodology using MSI IC's. Multiplexer, Demultiplexer (Trees), multi variable function implementation using MUX & decoder. Parallel adder (1C 7483). Look ahead carry generator, arithmetic logic unit (IC 74181).

Programmable Logic Devices: Detail architecture, study of PROM, P AL,

PLA, designing combinational circuits using PLDs.(Code conversion)

Unit-IV (09 Hours)

Sequential Logic Circuit:

Study of flip-flops, flip-flop truth table, 1 bit latch, SR flip-flop, Clocked SR flip-flop, JK flip-flop, Race around condition, Master-Slave JK flip-flop, D flip-flop, T flip-flop. Design of ripple counter using flip-flop (1 C 7490,93) 4 bit up/down (positive / negative edge triggered).

Shift register (modes of operation), 4 bit bi-directional using D/ J-K universal shift registers, application of shift registers (Ring counter, Sequence generator, Johnson's counter) IC 7495/74195.

Unit-V (07 Hours)

Synchronous Sequential Machines:

Design of Synchronous counter using lC 74191 ,4 bit up/down mod-n counters. Moore/Mealy M/C's, representation techniques, state diagrams, state tables, state reduction, state assignment, implementation using flip-flops. Applications like sequence generator and detection.

AID and D/A converters: Digital to Analog converters, example of D/ A converter 1 C, Analog to Digital converters, example of AID converter.

Unit-VI (07 Hours)

Semiconductor Memories:

Memory organization and operation, expanding memory size, classification and characteristics of memory, RAM, ROM, EPROM, EEPROM, NVRAM, SRAM, DRAM .

List of Practical

Verification of parameters & transfer characteristics of74LS and 74HC family.

I Verification of TTL - CMOS/CMOS- TTL interfacing.

Code conversion using logic gates: BCD to Binary, BCD to Gray, Gray to BCD 4. Design and implementation of 2 bit digital comparator using logic gates and

Functional verification of 4 bit digital comparator IC 7485.

Design & implementation of 1 digit BCD adder using IC 7483. 6. A) Verification of functionality of multiplexer and demultiplexer

a) Verification of functionality of multiplexer and demultiplexer Ics

b) Design and implement combinational function using multiplexer and demultiplexer

a) Design & implementation of 3 bit bi directional shift register using D flip flop

b) Design and implementation of Johnson counter using above shift register

a) Functional verification of universal shift registers IC 7495/194

b) Design and implementation of pulse train generator using above 1 C

Design and implementation of3 bit up down ripple counter using flip-flop

Functional verification of ripple counter IC 7490 & synchronous counter IC 74191(mod n operation)

Verification of DAC using R/2R method

Text Books/References

M. Morris Mano, "Digital Design", PHI (3rd Edition)

R.P. Jain, "Modern Digital Electronics", TMH

Tocci, "Digital Systems", (PHI)

Gothman, "Digital Electronics", (PHI)

Syllabus for Unit Test

Unit Test 1	Unit I & II
Unit Test 2	Unit III & IV
Unit Test 3	Unit V & VI

K50230: COMPUTER ORGANISATION AND OPERATING SYSTEMS

TEACHING SCHEME
Lectures : 04Hrs/week

EXAMINATION SCHEME
Theory : 80 Marks
Duration : 03 Hours
Unit Test : 20 Marks

Unit -I (07 Hours)

Structure Of A Computer System:

Brief History of computers, Von Neumann Architecture, Functional Units, Bus structures and Interconnection networks, Performance.

Control Unit Design: Machine Instructions and addressing modes, Single Bus CPU, Control Unit Operation: Instruction Sequencing, Micro-operations, (Register Transfer). Hardwired Control: Design methods, Design Examples: Multiplier CD. Micro-programmed Control: Basic concepts, Microinstruction-sequencing and execution, Micro-program control, Applications of microprogramming, Emulator.

Unit –II (09 Hours)

Central Processing Unit:

CPU Architecture, Intel IA-32 Family Architecture as an example, Register Organization, Addressing modes, Instruction types, instruction formats (Intel, Motorola processors), Instruction cycles, Instruction pipelining, Types of operands, Addressing Modes.

Memory Organization: Internal Memory, Characteristics of memory systems and Hierarchy, Chip Packaging, Main Memory, ROM, EPROM, RAM: SRAM, SDRAM, DRAM, RDRAM.

High-Speed Memories: Cache Memory, organization and Mapping, Replacement Algorithms, Cache Coherence, MESI protocol. Interleaved and Associative Memories, Virtual Memory: Main Memory allocation, Segmentation, paging.

Secondary Storage: Magnetic Disk, Tape, DA T, RAID, Optical memory, CDROM, DVD

Unit-III (08 Hours)

I/O Organization:

Input/Output Systems, Programmed I/O, Interrupt driven I/O, Traps, Faults, Exceptions, Pentium Interrupt Structure, I/O channels, Direct Memory Access, Standard Buses, Synchronous, Asynchronous, Parallel, Serial, PCI, SCSI, USB Ports.

Peripherals: Keyboard, Mouse, Scanners, Video Displays, Dot-Matrix, Desk-jet, Laser Printers.

Multiprocessor Configurations: Closely coupled and loosely coupled multiprocessor architectures, Problems of bus contentions, Interprocess Communications, Coprocessor and I/O Processor, Bus controller, Bus Arbitration, System Bus-Uni-Bus, Multibus.

Unit-IV (08 Hours)

Introduction to Operating System:

Architecture, Goals & Structures of O. S, Basic functions, Interaction of O. S. & hardware architecture, System calls & O. S. services. Batch, multiprogramming. Multitasking ,time sharing ,parallel ,distributed & real -time O. S. examples of O. S.: Linux and variants, MS-Windows, Handheld O. S.

Unit-V (09 Hours)

Process Management:

Process description & control: Process Concept, Process states, Process description, Process control, Threads

Concurrency: Principles of Concurrency, Mutual Exclusion: SIW approaches, HA V Support, Semaphores, Message Passing, Monitors.

Deadlock: Principles of deadlock, Deadlock Prevention, Deadlock Avoidance, Deadlock Detection, An Integrated Deadlock Strategies .

Scheduling: Uniprocessor Scheduling: Types of scheduling: Preemptive, No preemptive, Scheduling.

Multiprocessor Scheduling: Granularity, Design Issues, Process Scheduling, Thread Scheduling, Real Time Scheduling: Characteristics, Real Time Scheduling

Unit-VI (07 Hours)

Memory Management Software:

Memory Management requirements, Memory partitioning: Fixed and Variable Partitioning, Fragmentation, Swapping ,Paging.

Virtual Memory: Concepts, Segmentation, Paging, Address Translation, Demand paging, I/O

Devices & Files: I/O management &

Disk scheduling: I/O Devices, Organization of I/O functions, Operating System Design issues, I/O Buffering.

File Management: Concepts, File Organization, File Directories, File Sharing, Record Blocking, Free Space management, Security Issues Secondary Storage Management .

Text Books/References

C. Hamacher, V. Zvonko, S. Zaky, "Computer Organization", 5th Edition, McGraw Hill, 2002 ISBN 0 - 07 - 120411 - 3

Stalling William, "Operating Systems", Pearson Education, 2001, ISBN 81-7808503-8

W. Stallings William, "Computer Organization and Architecture: Principles of Structure and Function", 2nd Ed, Maxwell Macmillan Editions, 1990 ISBN 0 - 02 946297 - 5 (Chapter: 2,3,4,5,7,8,9,10,11,12,13,14)

A. Tanenbaum, "Structured Computer Organization", 4th Ed, Prentice Hall of India, 1991 ISBN 81 - 203 - 1553 -7 (Chapter: 1,4,5,6,8)

Nutt Gary, "Operating Systems", Pearson Education, 2004, ISBN 81-297-0614-8

Tanenbaum Andrew S.,"Modem Operating Systems" PHI, 2001.ISBN 81-203-0974-X

Syllabus for Unit Test

Unit Test 1	Unit I & II
Unit Test 2	Unit III & IV
Unit Test 3	Unit V & VI

K50231: SIGNALS AND SYSTEMS

TEACHING SCHEME		EXAMINATION SCHEME	
Lectures	: 04Hrs/week	Theory	: 80 Marks
Practical	: 02Hrs/week	Duration	: 03 Hours
		Unit Test	: 20 Marks
		T. W. & Or.	: 50 Marks

Unit -I (07 Hours)

Introduction To Signals:

Signals: Definition of signal, Classification of signals, Continuous and Discrete time, Analog & Digital, Periodic & Non-periodic, Deterministic and non-deterministic, Energy & power. Basic signals &Operations on signals, Sine, Cosine, Exponential and unit step, Unit Impulse. Even, Odd. Time shifting, time scaling, Differentiation and integration of signals.

Unit –II (09 Hours)

Classification of Discrete Time System:

Definition, Classification, Linear Nonlinear, Time variant and time invariant, Casual & Non-causal, Static & dynamic, Stability.

LTI system Analysis: Introduction to LTI systems. Block Diagram 7 System Terminologies. Convolution Integral. Impulse response. Convolution & Methods of Convolution. Properties of convolution, System interconnections, stability & impulse response of systems to standard signals.

Unit-III (08 Hours)

Continuous Time Analysis:

Response of LTI Systems to exponential signals, periodic signals. Fourier series, Fourier Transforms, properties, application of Fourier series & Fourier transforms to the system analysis.

Laplace Transforms: Definition and its properties, methods of inversion, application to LTI system analysis.

Unit-IV (09 Hours)

Correlation, Energy Spectral Density and Power Spectral Density:

Introduction, Correlation & Correlogram, The correlation function:

Conceptual basis, Energy signals, power signals, Auto- correlation: Relation to signal energy and signal power, properties of Auto-correlation.

Cross-correlation: Properties of cross-correlation,

Energy Spectral Density: Definition & Derivation of PSD, Effects of system on ESD, The PSD concept, Relation of ESD to auto-correlation, Power Spectral Density: Definition & derivation of PSD, Sampling Theorem and its roof, effects of under- sampling, sampling of band pass signals.

Unit-V (08 Hours)

Probability:

Sample space, Event, probability, Conditional Probability and statistical independence. Random Variables, Discrete Random variable, Cumulative Distributive Function, Continuous Random Variable, Probability Density Function, Properties of CDF and PDF.

Unit-VI (07 Hours)

Random Variables and Random Processes:

Transformation of random variables, Statistical averages, Mean, Moments and expectations. Probability models, Binomial, Poisson's Gaussian, Rayleigh.

Random Process: Ensemble averages ad correlation functions, Ergodic and stationary Process. Gaussian process. Random Signals, power spectral density, auto-correlation, Superposition and Modulation.

List of Practicals

Generation of Signals

Signal Convolution

Correlation- Auto & Cross

Laplace Transform

Inverse laplace Transform

Fourier Transform

Inverse Fourier Transform

PDF, CDF

Mean, Standard Deviation, Variance & Moments

Note: All the Practical's to be conducted using MATLAB

Text Books/References

Roberts MJ, "Signals & Systems", TMH

Oppenheim, Wilsely & Nawab, "Signals Systems", (MGH)

Syllabus for Unit Test

Unit Test 1	Unit I & II
Unit Test 2	Unit III & IV
Unit Test 3	Unit V & VI

RULES REGARDING ATKT, CONTINUOUS ASSESSMENT AND AWARD OF CLASS

A. T. K. T.

A candidate who is granted term for B.Tech. Semester-I will be allowed to keep term for his/her B.Tech. Semester-II examination even if he/she appears and fails or does not appear at B.Tech. Semester-I examination.

A candidate who is granted term for B. Tech. Semester - III will be allowed to keep term for his/her B.Tech. Semester-IV examination even if he/she appears and fails or does not appear at B.Tech. Semester-III examination.

A candidate who is granted term for B.Tech. Semester-V will be allowed to keep term for his/her B.Tech. Semester-VI examination if he/she appear and fails or does not appear at B.Tech. Semester-V examination.

A candidate who is granted term for B.Tech. Semester-VII will be allowed to keep term for his/her B.Tech. Semester-VIII examination if he/she appears and fails or does not appear at B.Tech. Semester-VII examination.

A student shall be allowed to keep term for the B.Tech. Semester-III course if he/she has a backlog of not more than 3 Heads of passing out of total number of Heads of passing in theory examination at B.Tch. Semester-I & II taken together.

A student shall be allowed to keep term for the B.Tech. Semester-V of respective course if he/she has no backlog of B.Tech Semester-I & II and he/she has a backlog of not more than 3 Heads of passing in theory examination and not more than 3 heads of passing in termwork and practical examination or termwork and oral examination.

A student shall be allowed to keep term for the B.Tech. Semester-VII course if he/she has no backlog of B.Tech. Semester-III & IV and he/she has a backlog of not more than 3 Heads of passing in theory examination and not more than 3 Heads of passing in termwork and practical examination or termwork and oral examination.

CONTINUOUS ASSESSMENT

In respect of Term work at B.Tech. Semester-I & II, B.Tech. Semester-III & IV and B.Tech. Semester-V & VI, target date shall be fixed for the completion of each job, project experiment or assignment as prescribed in the syllabus and the same shall be collected on the target date and assessed immediately at an affiliated college by at least one pair of the concerned teachers for the subject and the marks shall be submitted at the end of each term to the Principal of the college.

Termwork and performance of Practical/Oral examination shall be assessed on the basis of the depth of understanding of the principles involved, correctness of results and not on ornamental or colorful presentation.

For B.Tech. Semester-VII & VIII, termwork assessment will be done by external and internal examiners jointly during the examination schedule declared by the university. The record of continuous assessment shall be made available to the examiners during Term work and practical and Term work and oral examinations. Examiner shall use this record for overall assessment of the performance of the student. Every practical/termwork assignment shall be assessed on the scale of 20 marks and weightage of 20 marks shall be distributed as follows:

Sr. No.	Activity	Marks
1	Timely Submission	04
2	Presentation	06
3	Understanding	10

Marks obtained out of 20 for all assignments together will be converted on scale of marks assigned to term work of respective subject in the structure of the course.

CLASS

The class should be awarded to the student on the basis of aggregate marks obtained together in both the semesters of the respective year by him. The award of class shall be as follows.

A	Aggregate 66% or more marks	First Class with Distinction
B	Aggregate 60% or marks but less than 66%	First Class
C	Aggregate 55% or more marks but less than 60%	Higher Second Class
D	Aggregate 50% or more marks but less than 55%	Second Class
E	Aggregate 40% or more marks but less than 50%	Pass Class