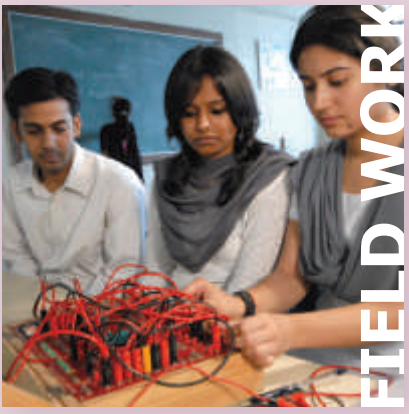
BHARATI VIDYAPEETH UNIVERSITY,
Pune.

(Established under Section 3 of UGC ACT 1956)

COURSE STRUCTURE AND SYLLABUS

B. Tech. (ELECTRONICS)
(Sem. III & IV)



COURSE STRUCTURE & SYLLABUS

BHARATI VIDYAPEETH UNIVERSITY, PUNE

B. Tech. (ELECTRONICS) (Sem. III & IV)

HIGHLIGHTS

Bharati Vidyapeeth University College of Engineering (BVUCOE) is the largest Engineering College in Maharashtra with an intake of 700 students in each academic year. Imparting quality technical education from Under Graduate to Doctorate Level, BVUCOE is probably the only Engineering College in India with an accreditation from both NAAC as well as NBA. The faculty at BVUCOE boasts of highly qualified academicians, a quality that is further emphasized by the fact that 15 of them are presently pursuing their Ph.D. degree.

BVUCOE has been ranked 29th amongst the Top 50 Technical Schools of India in survey conducted by DATAQUEST-IDC. We have enjoyed a ranking in this list for the last 4 years. Research is of utmost importance in all our programs. A total of 113 research papers were published in the academic year 2007-2008.

Currently we have 12 ongoing research projects. The infrastructure of BVUCOE is state-of-the-art with 62 classrooms, 59 laboratories and a well-stocked library that currently holds 27,130 titles. The college has an international presence with MoUs signed with the North Carolina A&T State University (Greensboro, USA), University of Venice (Italy), Actel Corporation (USA).Corporate interaction is also inculcated in our programs through our association with Oracle India Ltd., Infosys Ltd. and Tata Consultancy Services.

SALIENT FEATURES

India is the fourth largest telecom market in Asia. The Indian telecom market is eighth largest in the world and second largest among emerging economies. The industry has witnessed an explosive growth in the field of electronics in the recent years. India has institutions that are deeply rooted in the principles of democracy and Justice. This ensures a transparent, predictable and secure environment for development of electronics field.

The National Telecom policy 1999 (NT 99) targets tele-density at 15 per cent by 2010. The Indian market presents a unique opportunity as compared to developed countries, hence increasing the attractiveness of the Indian market.

In the engineering field, electronics branch is one of the most significant as it reflects today's changing technology. It has become a must-know field as it forms the base for all other engineering branches.

To comply with the present day requirements & keep pace with the recent technology, the course is designed to provide the students with technical know-how. The department therefore aims to ensure that the students excel in hardware as well as software technologies. The department has started post-graduate course leading to M.E. Electronics (VLSI) which focuses on the theory, design, implementation and application of this upcoming technology in technical context.

The department has received a grant of Rs. 45.5 Lakhs from UGC under their innovative program scheme to start the Biomedical Engineering course with the intake capacity of 40 students.

College has established collaboration with ACTEL Corporation, USA. Under this collaboration an advanced VLSI laboratory is established jointly. For this laboratory, ACTEL Corporation has provided software and hardware worth $3, 56,000 (Approx. 1.5 Crores)

The department has well-qualified and experienced staff with 6 Professors, 2 Assistant-Professors and 11 lecturers. Most of them have completed post-graduation and some are pursuing.

MAJOR GROUPS / AREAS

Image Processing, Digital Signal Processing, Very Large Scale Integration, Biomedical Engineering, Fiber optic sensors

EXPERTISE IN RESEARCH AND CONSULTANCY

Electronics engineering department received a grant of 6.5 lakhs from All India Council for Technical Education (AICTE), New Delhi for development of DSP laboratory under MODROB scheme. Research has been carried out in the field of signal

processing, control and communication with credit of five research papers published at national level. Three staff members are pursuing PhD work in the field of signal processing and communication. The department has received the grant of Rs. 70, 000 from Institute of Engineers, Pune for various research projects undertaken by students.

MAJOR EQUIPMENT

Mixed Signal Oscilloscope, Vector Voltmeter, Digital Storage Oscilloscope, Wobbuloscope, Powerscope, Allen-Bradley PLC with RSLogix500 software, Ratio Control Unit Trainer, ICAP 4, DSP Processor Training Boards & EVMs, X-ray machine (Demo type), Ultrasound scanner (Demo type), Blood cell counter, EEG hardware and software, Spectrophotometer (Demo type), Gas chromatography system (Demo type), ECG stress test software with thread mill

SOFTWARE

ORCAD, XLINX 3.1, Altera, MATLAB, LabView, ALDEC, Code Composer Studio, Libero

LABORATORIES

ACTEL-VLSI Lab, Microelectronics Laboratory, Digital Electronics Laboratory, Network and Lines Laboratory, Electric Circuit Design and Project Laboratory, Communication Laboratory, Microprocessor and Microcontroller Laboratory, Computer Networking Laboratory, DSP and Image Processing Laboratory, Electronic Instrumentation and Measurements, Power Electronics Laboratory, Instrumentation and Control Laboratory, Biomedical Laboratory, Computer Lab

B. Tech. - Electronics Engineering

Semester III

Total Duration : 28 hours/week
Total Marks : 750

Subject Code	Subject	Teaching Scheme (Hrs.)		Examination Scheme (Marks)				Total (Marks)
		L	P	Theory	Unit Test	TW & Pr	TW & Or	
K50201	Electronic Devices & Circuits	04	02	80	20	50	50	200
K50202	Network Analysis	04	02	80	20	50	-	150
K50203	Fundamentals of Instrumentation & Control	04	02	80	20	-	50	150
K50204	Computational Techniques	04	02	80	20	-	50	150
K70201	Engineering Mathematics-III	04	-	80	20	-	-	100
	Total	**20**	**08**	**400**	**100**	**100**	**150**	**750**

Teaching Scheme		Examination Scheme				Total
Lectures	Practical	Theory	Unit Test	T.W. & Pr.	T.W. & Or.	
20	08	400	100	100	150	750

Semester IV

Total Duration : 28 hours/week
Total Marks : 750

Subject Code	Subject	Teaching Scheme (Hrs.)		Examination Scheme (Marks)				Total (Marks)
		L	P	Theory	Unit Test	TW & Pr	TW & Or	
K50207	Electronic Circuits	04	02	80	20	50	50	200
K50208	Analog Communications	04	02	80	20	50	-	150
K50209	Digital Electronics & Logic Design	04	02	80	20	50	-	150
K50210	Linear Integrated Circuits	04	02	80	20	50	-	150
K50211	Signals & Systems	04	-	80	20	-	-	100
	Total	**20**	**08**	**400**	**100**	**200**	**50**	**750**

Teaching Scheme		Examination Scheme				Total
Lectures	Practical	Theory	Unit Test	T. W. & Pr.	T. W. & Or.	
20	08	400	100	200	50	750

RULES FOR CONDUCTING TESTS

Mode of the test

In each semester for each subject three tests shall be conducted. The schedule for the same will be declared at the commencement of academic year in the academic calendar.

Each test shall carry 20 marks.

University examination pattern has given weightage of 20 marks for the tests.

To calculate these marks following procedure is followed:

i) Out of the three tests conducted during the semester, the marks of only two tests in which the candidate has shown his/her best performance shall be considered, to decide the provisional marks in each subject.

ii) Average marks obtained in two tests in which students have performed well, shall be considered as provisional marks obtained by the student in the tests.

iii) If the candidate appears only for two tests conducted during the semester, he/ she will not be given benefit of the best performance in the tests.

iv) If the candidate appears only for one test conducted during the semester, to calculate the marks obtained in the tests it will be considered that the candidate has got 0 (zero) marks in other tests.

v) The provisional marks obtained by the candidate in class tests should reflect as proportional to theory marks. In cases of disparity of more than 15% it will be scaled down accordingly; These marks will be final marks obtained by the student. No scaling up is permitted.

vi) If the candidate is absent for theory examination or fails in theory examination his final marks for tests of that subject will not be declared. After the candidate clears the theory, the provisional marks will be finalized as above.

Paper Pattern for Tests

i) All questions will be compulsory with weightage as following

Question 1	-	7 marks
Question 2	-	7 marks
Question 3	-	6 Marks

ii) There will not be any sub-questions.

For granting the term it is mandatory to appear for all the three tests conducted in each semester.

Roll numbers allotted to the students shall be the examination numbers for the tests.

SEMESTER - III

K50201: ELECTRONIC DEVICES & CIRCUITS

TEACHING SCHEME		EXAMINATION SCHEME	
Lectures	: 04 Hrs/week	Theory	: 80 Marks
Practical	: 02 Hrs/week	Duration	: 03 Hours
		Unit Test	: 20 Marks
		T. W. & Pr	: 50 Marks
		T. W. & Or	: 50 Marks

Unit-I (08 Hours)

Study Of Electronic Materials & Components:

Classification of materials based on band gaps; Semiconductors materials Si, Ge. Types of Resistors : 1. Fixed 2. Variable 3.Precision etc.

Like carbon film, metal film, wire wound, their standard values, specifications and applications. Classification of capacitors based on dielectrics, standard values, specifications & applications of capacitors, types of capacitors – electrolytic ceramic, paper, mica, tantalum, plastic film etc. Study of different core materials depending on range of frequencies - for inductors & transformers.

Unit-II (09 Hours)

Semiconductor Diode Characteristics:

Diffusion phenomenon, concentration gradient, Einstein relation, volt equivalent of temperature, total current (drift & diffusion), potential variation within continuous and step graded semiconductor p-n junction. Current components in forward biased/reverse biased p-n junction diode, cut in voltage, reverse saturation current. Characteristics (Logarithmic) equation of diode temperature dependence of diode characteristics concepts and significance & expressions of transition and diffusion capacitance, junction diode switching times.

Unit-III (08 Hours)

Application Of Semiconductor Diode:

Diode as rectifier, half wave, full wave and bridge rectifier with and without capacitor & filter, different types of filters-L-section and Π section input Parameters like ripple factor efficiency, TUF, PIV, I Imax, I surge, etc. Derivation of ripple factor for L, C and L section filter, Π section. bleeder resistor. Diode as a wave shaping element in clipping and clamping circuits, voltage multipliers.

Unit-IV (09 Hours)

BJT (Bipolar Junction Transistor):

(07 Hours)

(07 Hours)

Millman & Halkias, Integrated Electronics, Mc Graw Hill

Millman & Halkias, Electronic Devices & Circuits, Mc Graw Hill

Syllabus for Unit Test

Unit -I

Error Analysis & Roots Of Polynomial:

Sources , types, analysis . Bisection method , Regula falsi method , Newton Raphson, Secant , iterative , convergence tests.

Unit –II

Interpolation/Optimization:

Finite difference operators , interpolation techniques based on finite differences, Newton's forward, backward, divided . Lagrange's, spline, least squares.

Unit-III

Linear Equations & Numerical Integration:

Gauss Jordan, Gauss Elimination , Jacobis , Gauss Siedel, LU decomposition, analysis of methods

Trapezoidal, Simson's 1/3 & 3/8 rules .

Unit-IV

Differential Equations & Monte Carlo Techniques:

Taylor's series, Euler's method, Runge Kutta 4th order, predictor corrector & stability analysis . Simulation for integration , pseudo random nos.

Unit-V

Searching & Sorting:

Sorting: Bubble, Quick , Insertion , Selection , Shell , Merge , Radix , analysis. Searching: Sequential , Binary , Hashing.

Unit-VI

Data Structures:

Unit Test 1	Unit I & II
Unit Test 2	Unit III & IV
Unit Test 3	Unit V & VI

K50202: NETWORK ANALYSIS

TEACHING SCHEME		EXAMINATION SCHEME	
Lectures	: 04 Hrs/week	Theory	: 80 Marks
Practical	: 02 Hrs/week	Duration	: 03 Hours
		Unit Test	: 20 Marks
		T. W. & Pr.	: 50 Marks

Unit -I (09 Hours)

Network Techniques & Theorem:

Network definition, mesh & node analysis, principle of duality, source transformation, Simplification of networks. T & it conversion. Twin T & Wienbridge networks. Super position theorem, Thevenins theorem, Norton's theorem, Reciprocity theorem , Millman's theorem, Maximum power transfer theorem.

Unit –II (09 Hours)

Transients & Resonance:

Undriven & driven RC, RL, RLC circuit. initial conditions.

Figure of merit, conditions for resonance, various properties of series & parallel resonance.

Unit-III (08 Hours)

Two Port Network:

Various types of four terminal network:, defin4tion of characteristic impedance (Zo), propagation constant, image impedance , iterative impedance, calculation of above parameter.

Unit-IV (08 Hours)

Filters (Passive):

Filter fundamentals , LPF , HPF , BPF , BSF , prototype(constant k) & m - derived filters , composite filters.

Unit-V (07 Hours)

Network Functions:

Terminals & terminal pairs , network function, poles & zeros and its significance.

Z, Y, H, A B C D parameters, Equivalent circuit , inter relationship between parameters, interconnection of two port network, Study of ideal transformer.

Unit-VI (07 Hours)

Network Synthesis:

Positive real function, properties of LC, RL, R driving point function. Realization of positive real function in four canonical form for one port network.

List of Practicals

Network Theorems -I: Thevenin's & reciprocity theorem.

Network Theorem-II: Superposition & maximum power transfer theorem.

Filter-I: Low pass filter & High pass filter.

Filter-II: Band pass filter & band stop filter.

Resonance: Series and Parallel .

Transient response of RLC circuit.

Z & Y Parameters.

h & ABCD Parameters.

Step and Impulse response of given network using MATLAB.

Any two assignments using PSPICE or any software. Experiment can be set on filters transient response or theorem .

Text Books/References

Van Valkenberg , "Linear Circuit".

D.Roy Choudhary, "Network Analysis & Synthesis", PHI.

John O'Malley, " Basic Circuit Analysis", Schaum's series 2nd Ed.

Franklin Kuo , "Network Analysis & Synthesis".

Syllabus for Unit Test

Unit Test 1	Unit I & II
Unit Test 2	Unit III & IV
Unit Test 3	Unit V & VI

K50203: FUNDAMENTALS OF INSTRUMENTATION & CONTROL

TEACHING SCHEME		EXAMINATION SCHEME	
Lectures	: 04 Hrs/week	Theory	: 80 Marks
Practical	: 02 Hrs/week	Duration	: 03 Hours
		Unit Test	: 20 Marks
		T. W. & Or	: 50 Marks

Instrumentation Control Devices: (09 Hours)

Control actions: On/Off, P, PI, PD, PID. PLC: Architecture, comparison with relay logic. Ladder Diagrams for simple applications

List of Practicals

Unit step and ramp response of the transfer function system using MATLAB.
To draw Root locus and Bode plot using MATLAB.
Magnitude and phasor plot of lead network.
Magnitude and phasor plot of lag network. (07 Hours)
Transient response of second order system.
To Study characteristic of temperature transducer
To Study the characteristics of LVDT for displacement measurement
Flow control using Proportional controller action.
Verification of ladder diagram using PLC
Study of I/P converter

(08 Hours)

Text Books/References

Nagrath and Gopal, Control Systems

A.K.Sawhney, Electrical & Electronic Measurements & Instrumentation, Dhanpat Rai & Co Ltd.

(09 Hours)

H. S. Kalsi, Electronic Instrumentation, Tata McGraw Hill

K. Ogata, Modern Control Engineering

Syllabus for Unit Test

Unit -I

Basics For Electronic Communication: (08 Hours)

Properties of sound, Types of microphones and loudspeakers, encloures, Different methods of sound recording and reproduction (Analog &

digital sound) Monophony , Stereophony P.A. system & Hi-Fi system. (07 Hours)
Types of noise, Noise calculation, Noise figure, Noise temperature.

Unit Test 1	Unit I & II
Unit Test 2	Unit III & IV
Unit Test 3	Unit V & VI

K50204: COMPUTATIONAL TECHNIQUES

TEACHING SCHEME		EXAMINATION SCHEME	
Lectures	: 04 Hrs/week	Theory	: 80 Marks
Practical	: 02 Hrs/week	Duration	: 03 Hours
		Unit Test	: 20 Marks
		T. W. & Or	: 50 Marks

Queues, Stacks, linked lists & Binary trees. (08 Hours)

List of Practical

Minimum of one assignment on each topic should be conducted in C. It will cover algorithm ,error analysis and C program implementation.

(08 Hours)

Text Books/References

Gere J. M. & Timoshenko S. P., Numerical Methods for Scientific Engineering & Computation, New Age Int'l

Chapra & Canale, Numerical Methods for Engineers, Tata McGraw Hill

Willian Press, Numerical Receipes in C, Oxford Press

(09 Hours)

Syllabus for Unit Test

Unit -I

Linear & Non-Linear Control System:

Introduction to linear & nonlinear control system, Elements of control systems, Open loop & closed loop, feedback & feed forward control systems. (Each control systems will be highlighted with real time applications). Transfer function using block diagram reduction techniques & signal flow graph using Mason's gain formula. (09 Hours)

Unit –II (07 Hours)

Transient Response:

Time domain Analysis of linear control systems. First order & second order system. Error constant, steady state error, transient response specifications. Stability of control system, Routh-Hurwitz criterion and Root locus technique.

(07 Hours)

Unit-III

Frequency Domain Analysis:

Frequency domain analysis frequency domain specification, Bode plot-Gain margin and phase margin, Mapping theorem and Nyquist Plot.

Unit-IV

Transducers:

Characteristics, types of transducers for temperature (RTD, Thermocouple, Thermistor), Capacitance type level, electromagnetic type flowmeter, pressure transducer, LVDT, Strain gauge, piezoelectric type accelerometer, photoelectric tachometer (Pick up)

Unit-V

Signal Conditioning:

Signal conditioning circuits, for above transducers, study of synchros.

Unit-VI

Unit Test 1	Unit I & II
Unit Test 2	Unit III & IV
Unit Test 3	Unit V & VI

K70201: ENGINEERING MATHEMATICS-III

TEACHING SCHEME
Lectures : 04 Hrs/week

EXAMINATION SCHEME
Theory : 80 Marks
Duration : 03 Hours
Unit Test : 20 Marks

Unit-I (09 Hours)

Differential Equations:

Solution of Linear differential equation of n^{th} order with constant coefficients, Method of variation of parameters, Cauchy's and Legendre's linear equations, Simultaneous linear differential equations, Total differential equations, Symmetrical simultaneous differential equations. Applications to Electrical circuits.

Unit-II (08 Hours)

Complex Variables:

Function of complex variables, Analytic function, Cauchy–Riemann equations, Conformal mapping, Bilinear transformation, Residue theorem, Cauchy's Integral theorem and Cauchy's Integral formula.

Unit-III (09 Hours)

Transforms:

Fourier Transform: Fourier integral theorem, Fourier sine and cosine integrals, Fourier transform, Fourier sine and cosine transforms, Inverse Fourier transforms, Discrete Fourier transform and its applications.
Z -Transform: Definition, Properties, Inverse Z-Transform, Applications to difference equation, Relationship between Z-Transform and Fourier Transform.

Unit-IV (09 Hours)

Laplace Transform:

Definition, Properties and Theorems, Inverse Laplace transform, Methods of finding Inverse Laplace transforms, Laplace transform of Unit-step function, Dirac-delta functions, Periodic functions, Ramp functions, Error function, First order Bessel's function, Si(t), Ci(t), Ei(t). Applications to solution of linear differential equations.

Unit-V (09 Hours)

Vector Differentiation:

Vector Differentiation, Gradient, Divergence and Curl, Directional derivative, Vector identities, Irrotational and Solenoidal vector fields.

Unit-VI (08 Hours)

Vector Integration:

Line integral, Surface integral and Volume integral, Work done, Gauss-Divergence theorem, Stoke's theorem and Green's lemma, Applications to Electromagnetic fields.

Text Books/References

Peter V. O'Neil, Advanced Engineering Mathematics, 5e, Thomson Learning

Erwin Kreyszig, Advanced Engineering Mathematics, Wiley Eastern Ltd.

Wylie C. R. and Barrett L. C., Advanced Engineering Mathematics, McGraw-Hill

M. D. Greenberg, Advanced Engineering Mathematics, 2e, Pearson Education

B. S. Grewal, Higher Engineering Mathematics, Khanna Publication, Delhi

P. N. Wartikar and J. N. Wartikar, Applied Mathematics (Volume I & II), Pune Vidyarthi Griha Prakashan

Murray R. Spiegel, Laplace Transforms, Schaum's Outline Series– International Ed.

Syllabus for Unit Test

Unit Test 1	Unit I & II
Unit Test 2	Unit III & IV
Unit Test 3	Unit V & VI

SEMESTER - IV

K50207: ELECTRONIC CIRCUITS

TEACHING SCHEME		EXAMINATION SCHEME	
Lectures	: 04 Hrs/week	Theory	: 80 Marks
Practical	: 02 Hrs/week	Duration	: 03 Hours
		Unit Test	: 20 Marks
		T. W. & Pr.	: 50 Marks
		T. W. & Or.	: 50 Marks

(09 Hours)

Unit-VI

RF/HF Amplifiers:

Hybrid - small signal model of BJT, its relation with h-parameters, definitions of f, f, ft, calculation of Ai, Av, with finite load and source resistances for CE stage, Gain bandwidth product, Tuned load, loaded & unloaded Q, insertion loss, single tuned amplifiers, staggered tuning, cascade configuration for HF amplification .

List of Practicals

Analysis of multistage LF amplifier using BJT / FET, verification with theoretical values of Ais , Avs , Ri , Ro (overall) with square wave testing and comment on the results. Compute the simulation of above circuits.

Input impedance improvement techniques for emitter follower.

Biasing analysis of BJT power amplifier in class A, B, AB, C.

Calculation of efficiency & measurement of total harmonic distortion of class B/AB complementry symmetry power amplifier, verify the results using simulation. (07 Hours)

Analysis of LF amplifier with negative feedback in voltage & current series topology

Measurement of frequency of oscillation for op-amp based RC oscillators, BJT/FET based LC oscillators, crystal oscillators.

Linear applications of Op-Amp such as summing, difference, voltage follower, signal phase shifter.

Regulation characteristics of series & shunt regulators and calculation of Sv and Ro (Discrete)

IC 723 as basic high / low voltage regulator with simple / foldback current limiting. Design, build and test for given specification. (08 Hours)

Text Books/References

Thomas L. Floyd, Electronic Devices, Pearson Education (Sixth edition)

Millman & Halkis, Electronic Devices & Circuits, PHI

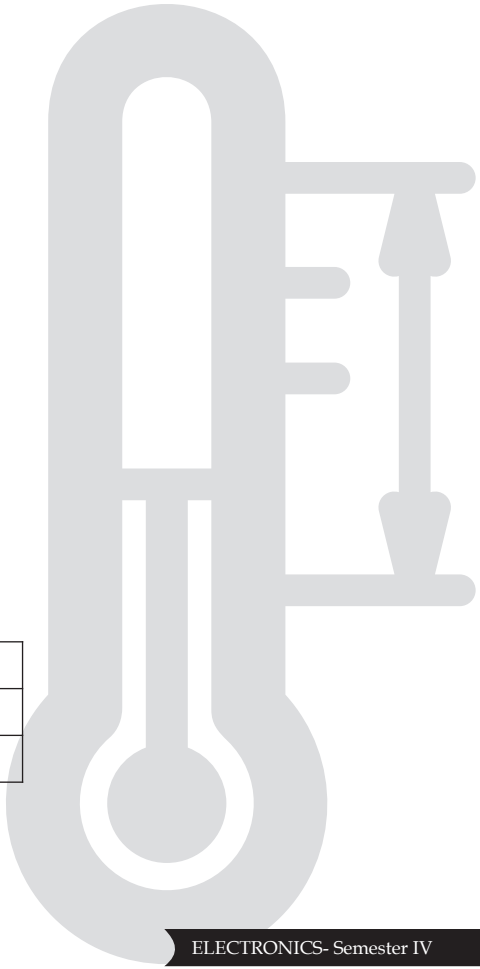
Millman & Halkis, Integrated Electronics, MGH

(08 Hours)

(08 Hours)

(09 Hours)

Unit Test 1	Unit I & II
Unit Test 2	Unit III & IV
Unit Test 3	Unit V & VI



K50208: ANALOG COMMUNICATIONS

TEACHING SCHEME		EXAMINATION SCHEME	
Lectures	: 04 Hrs/week	Theory	: 80 Marks
Practical	: 02 Hrs/week	Duration	: 03 Hours
		Unit Test	: 20 Marks
		T. W. & Pr	: 50 Marks

Frensel, Fundamentals of Communication, TMH (09 Hours)

R. G. Gupta, Audio video Engineering Systems, TMH

Syllabus for Unit Test

Unit -I

Number Systems And Coding: (08 Hours)

Number systems, Binary, Octal, Hexadecimal, Conversion methods, Binary addition and subtraction , 1's & 2's complement method. Concept of coding, BCD codes, 8421, Excess –3, Grey code , codes with more than four bits, ASCII code.

Unit –II

Design Methods: (08 Hours)

De-Morgan's theorem, Canonical and standard forms, dependency notation, minimization of logic functions, Karnaugh map upto 4 variables, SOP and POS forms, Don't care conditions, Quine Mc-Clusky method, multiple output minimization.

Unit-III

Logic Families And Semiconductor Memories: (07 Hours)

Logic Families TTL NAND gate, specifications, tristate TTL, bus organized computer principle, ECL, MOS, CMOS families and their interfacing in details. Semiconductor Memories: RAM, ROM, PROM, EPROM, EEPROM, NVRAM, SRAM, DRAM; Concept of PLA, PAD.

(09 Hours)

Unit-IV

Combinational Logic:

Code conversion , arithmetic circuits , Half and Full adder, subtractor, Binary Serial, Parallel Adder, IC 7483, BCD Adder, Excess-3 Adder,

Digital comparator.

Unit-V

Multiplexer And Demultiplexer:

Multiplexer, Demultiplexer, Encoder, Decoder and their applications, Design of ALU . (07 Hours)

Unit-VI

Sequential Logic Circuits:

S-R, Clocked S-R , JK and Master Slave JK flip flops , Flip –flop conversion, edge triggered flip-flops, design of Algorithmic State Machines (ASM) for simple applications.Design of ripple and synchronous counters, shift registers and pulse train generators, Pseudo Random Binary Sequencing (PRBS) generator, Analysis of chocked sequential circuits.

List of Practicals

Implementation of Boolean functions using logic gates

Study of characteristics of typical 74 TTL / 74 CMOS family like: fan in, fan out standard oad , noise margin & interfacing with other families

Half, Full Adder and subtractor using gates and IC's

Code conversion using digital IC's

2 bit digital comparator and ALU verification

Function implementation using Multiplxer and Demultiplexer

Sequence generator using MSJK flip flop IC's

Study of counters : Ripple , Synchronous , Ring , Johnson , Up-down counter and its application

Study of shift registers : Shift left , Shift right , parallel loading and Pulse Train generator

BCD Adder/Subtractor with Decoder driver and 7 segment display

Study of typical RAM IC.

Text Books/References

Gothman, Digital Electronics – An Introduction to Theory and Practice, PHI

Unit Test 1	Unit I & II
Unit Test 2	Unit III & IV
Unit Test 3	Unit V & VI

K50209: DIGITAL ELECTRONICS & LOGIC DESIGN

TEACHING SCHEME		EXAMINATION SCHEME	
Lectures	: 04 Hrs/week	Theory	: 80 Marks
Practical	: 02 Hrs/week	Duration	: 03 Hours
		Unit Test	: 20 Marks
		T. W. & Pr.	: 50 Marks

R .P . Jain, Modern Digital Electronics, TMH (09 Hours)

Tocci, Digital Systems-Principles & Applications, PHI

Douglas Hall, Digital Circuits and Systems, McGraw Hill

Syllabus for Unit Test

(08 Hours)

Unit -I

Frequency Amplifiers (BJT/FET):

Necessity of cascading LF small signal amplifiers in various configuration , techniques for improving input impedance of CC stage (Darlington connection , Bootstrapping) , CE-CE cascade , CE-CB cascade arrangement, effect of cascading on frequency response of single stage and cascaded amplifiers , square wave testing or step response of AF amplifier . (08 Hours)

Small signal LF- h parameter model in CE/CB/CC configuration : concept of A.C equivalent circuit of single stage amplifier, need of coupling and bypass capacitors; analysis CE/CB/CC amplifier for AI, AV, RI, & RO in terms of h- parameter. Simplified h-parameter model , effect of biasing and source resistance on performance of single stage amplifier, concept of frequency response.

(07 Hours)

Unit –II

LF Amplifiers With Negative Feedback:

Block schematic of amplifier with negative feedback , gain with feedback, consequences of introducing negative feedback in small signal and multistage amplifier , classification of amplifiers in view of feedback concept i.e. Ai, Av, Gm, Rm, types of sampling and mixing, ways of introducing negative feedback in amplifiers i.e. voltage series & shunt, (07 Hours)

current series & shunt and effect on Ri & Ro in all four types, Methodology of feedback amplifier analysis .

Unit-III (09 Hours)

Operational Amplifiers:

Internal block schematic of monolithic op-amp IC, Analysis of transistorized difference amplifier stage, Methods of improving CMRR, Definitions and measurement of op-amp parameters like input offset voltage and current, bias current CMRR, PSRR, open loop gain, etc., concept of dc amplification, inability of op-amp to work as a linear small signal amplifier in open loop, op-amp with closed loop negative feedback, closed loop gain and frequency response of op-amp, Linear applications like inverting & non – inverting amplifier, summing, difference.

Unit-IV

Large Signal (Power) Amplifiers:

Classification of amplifiers in class A, B, C, etc., concept of large signal amplification total harmonic distortion, push-pull configuration, efficiency of power conversion, CE transformer coupled amplifier, complementary symmetry CC power amplifier in single & dual supply version, efficiency and distortion analysis of those configuration (Graphical techniques to calculate harmonic distortion), cross over distortion, SOA and its limits, secondary breakdown, Heat sinks: standard shapes & sizes, thermal calculations and resistances and its calculations.

Unit-V

Oscillators & Voltage Regulators:

Employing positive feedback in amplifier, problems of instability, Barkhausen criteria for sinusoidal oscillators, derivation & analysis of transistorised RC phase shift / Wein Bridge for frequency expressions and gain requirements, LC oscillators: Hartley, Colpitts, Clapp, Crystal (Miller & Pierce), UJT relaxation oscillator, gain and frequency stability.

Zener diode as shunt regulator, emitter follower regulator, transistorised feedback type regulator, comparison of above discrete regulators on the basis of Sv, St, & Ro, CV / CC modes, over voltage & current protection circuits, internal block diagram, pin diagram and specification of

regulator its applications, SOA of IC regulators .

Unit Test 1	Unit I & II
Unit Test 2	Unit III & IV
Unit Test 3	Unit V & VI

K50210: LINEAR INTEGRATED CIRCUITS

TEACHING SCHEME

Lectures : 04 Hrs/week
Practical : 02 Hrs/week

EXAMINATION SCHEME

Theory : 80 Marks
Duration : 03 Hours
Unit Test : 20 Marks
T. W. & Practical : 50 Marks

(07 Hours)

(08 Hours)

(09 Hours)

(08 Hours)

(09 Hours)

(07 Hours)

Unit Test 1	Unit I & II
Unit Test 2	Unit III & IV
Unit Test 3	Unit V & VI

K50211: SIGNALS AND SYSTEMS

TEACHING SCHEME
Lectures : 04Hrs/week

EXAMINATION SCHEME
Theory : 80 Marks
Duration : 03 Hours
Unit Test : 20 Marks

(07 Hours)

(09 Hours)

(08 Hours)

(09 Hours)

(08 Hours)

(07 Hours)

Unit Test 1	Unit I & II
Unit Test 2	Unit III & IV
Unit Test 3	Unit V & VI

RULES REGARDING ATKT, CONTINUOUS ASSESSMENT AND AWARD OF CLASS

A. T. K. T.

A candidate who is granted term for B.Tech. Semester-I will be allowed to keep term for his/her B.Tech. Semester-II examination even if he/she appears and fails or does not appear at B.Tech. Semester-I examination.

A candidate who is granted term for B. Tech. Semester - III will be allowed to keep term for his/her B.Tech. Semester-IV examination even if he/she appears and fails or does not appear at B.Tech. Semester-III examination.

A candidate who is granted term for B.Tech. Semester-V will be allowed to keep term for his/her B.Tech. Semester-VI examination if he/she appear and fails or does not appear at B.Tech. Semester-V examination.

A candidate who is granted term for B.Tech. Semester-VII will be allowed to keep term for his/her B.Tech. Semester-VIII examination if he/she appears and fails or does not appear at B.Tech. Semester-VII examination.

A student shall be allowed to keep term for the B.Tech. Semester-III course if he/she has a backlog of not more than 3 Heads of passing out of total number of Heads of passing in theory examination at B.Tch. Semester-I & II taken together.

A student shall be allowed to keep term for the B.Tech. Semester-V of respective course if he/she has no backlog of B.Tech Semester-I & II and he/she has a backlog of not more than 3 Heads of passing in theory examination and not more than 3 heads of passing in termwork and practical examination or termwork and oral examination.

A student shall be allowed to keep term for the B.Tech. Semester-VII course if he/she has no backlog of B.Tech. Semester-III & IV and he/she has a backlog of not more than 3 Heads of passing in theory examination and not more than 3 Heads of passing in termwork and practical examination or termwork and oral examination.

CONTINUOUS ASSESSMENT

In respect of Term work at B.Tech. Semester-I & II, B.Tech. Semester-III & IV and B.Tech. Semester-V & VI, target date shall be fixed for the completion of each job, project experiment or assignment as prescribed in the syllabus and the same shall be collected on the target date and assessed immediately at an affiliated college by at least one pair of the concerned teachers for the subject and the marks shall be submitted at the end of each term to the Principal of the college.

Termwork and performance of Practical/Oral examination shall be assessed on the basis of the depth of understanding of the principles involved, correctness of results and not on ornamental or colorful presentation.

For B.Tech. Semester-VII & VIII, termwork assessment will be done by external and internal examiners jointly during the examination schedule declared by the university. The record of continuous assessment shall be made available to the examiners during Term work and practical and Term work and oral examinations. Examiner shall use this record for overall assessment of the performance of the student. Every practical/termwork assignment shall be assessed on the scale of 20 marks and weightage of 20 marks shall be distributed as follows:

Sr. No.	Activity	Marks
1	Timely Submission	04
2	Presentation	06
3	Understanding	10

Marks obtained out of 20 for all assignments together will be converted on scale of marks assigned to term work of respective subject in the structure of the course.

CLASS

The class should be awarded to the student on the basis of aggregate marks obtained together in both the semesters of the respective year by him. The award of class shall be as follows.

A	Aggregate 66% or more marks	First Class with Distinction
B	Aggregate 60% or marks but less than 66%	First Class
C	Aggregate 55% or more marks but less than 60%	Higher Second Class
D	Aggregate 50% or more marks but less than 55%	Second Class
E	Aggregate 40% or more marks but less than 50%	Pass Class