BHARATI VIDYAPEETH
(DEEMED TO BE UNIVERSITY), PUNE

Faculty of Engineering And Technology
M.Tech. - Electronics
New Syllabus

Bharati Vidyapeeth Deemed University,
College of Engineering, Pune
Structure of M.Tech (Electronics -VLSI) (Revised))
Based on Credit Pattern

Semester III									**Total Duration: 28 hrs/week** **Total Marks : 475** **Total Credits: 40**		
Subject	**Teaching Scheme (Hrs)** **Hrs./Week**		**Examination Scheme**						**Examination Scheme** **(Credits)**		**Total Credits**
	L	**P**	**Theory**	**Unit Test**	**Attendance**	**Tutorial/ assignments**	**TW**	**Pract/ Oral**	**TH**	**TW/PR /OR**	
Elective –I	04	02	60	20	10	10	25	25	04	01	05
Elective –II	04	02	60	20	10	10	25	25	04	01	05
**Self-Study Paper-I	* 04	--	60	20	10	10	-	-	04	-	04
Dissertation Stage –I	-	07	-	-	---	--	25	--		21	21
Seminar	-	05	-	-	--	--	25	25	-	05	05
Total	**12**	**16**	**180**	**60**	**30**	**30**	**100**	**75**	**12**	**28**	**40**

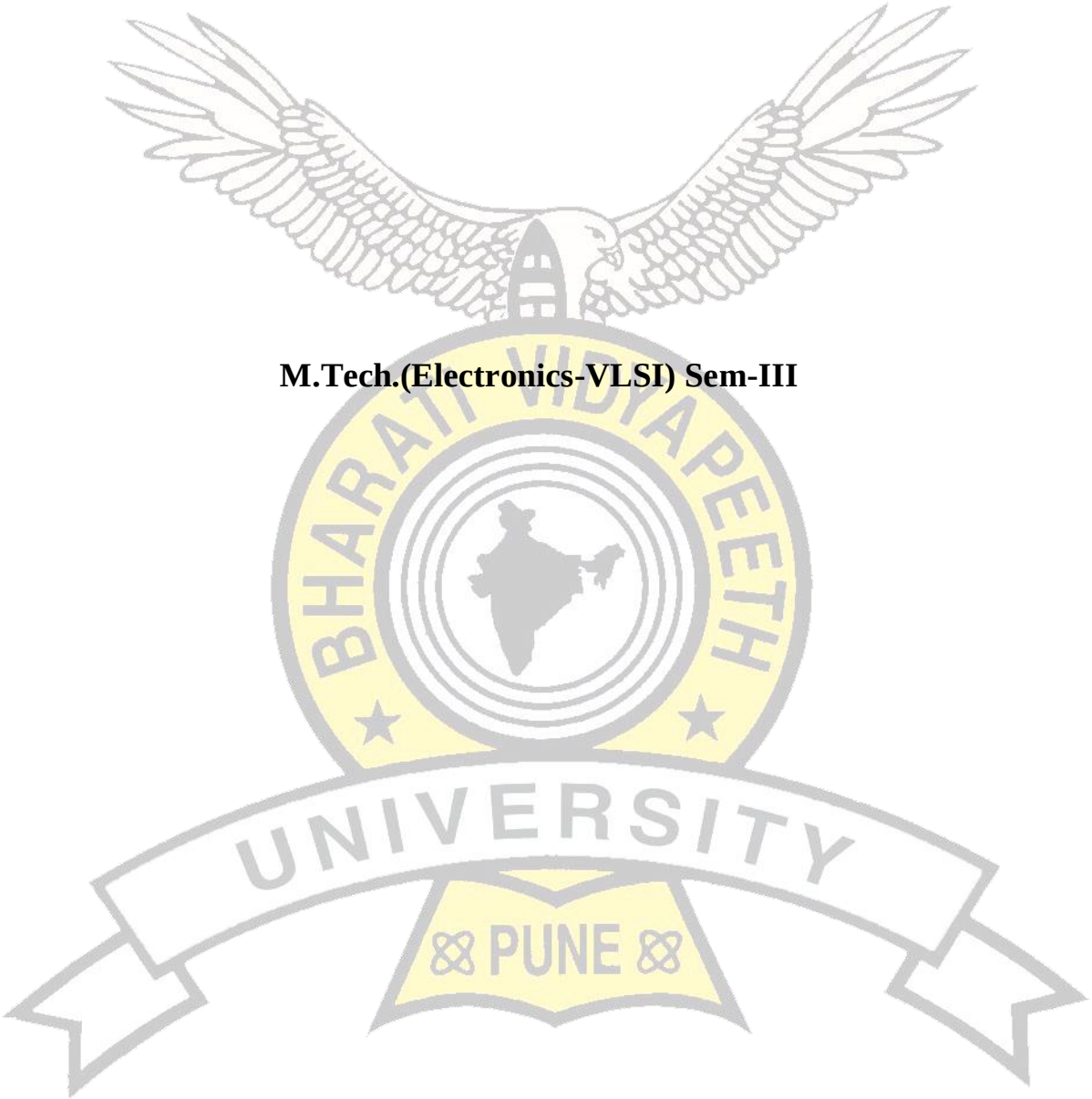
Elective – I	**Elective – II**
• Programmable System on chip • Nanoelectronics • Algorithms for VLSI Design Automation • Advanced Digital System design	• ASIC Design • Testing & Verification of VLSI Design • Artificial neural networks

Semester IV	**Total Duration: 14 hrs/week** **Total Marks : 325**

											Total Credits: 34
Subject	**Teaching Scheme (Hrs) Hrs./Week**		**Examination Scheme**						**Examination Scheme (Credits)**		**Total Credits**
	L	**P**	**Theory**	**Unit Test**	**Attendance**	**Tutorial/ assignments**	**TW**	**Pract/ Oral**	**TH**	**TW/PR /OR**	
**Self-Study Paper-II	* 04	--	60	20	10	10	-	-	04	-	04
Dissertation Stage –II	-	10	-	-	--	-	150	75		30	30
Total	**04**	**10**	**60**	**20**	**10**	**10**	**150**	**75**	**04**	**30**	**34**

List of Self Study Subjects

Sr. No.	SELF STUDY PAPER- I (SEM-III)	SELF STUDY PAPER- II (SEM-IV)
1	Low power VLSI Design	Genetic algorithms & optimization techniques
2	IC Fabrication Technology	Fuzzy Logic systems
3	In-Vehicle Networking	Biomedical Instrumentation
4	Research methodology	Computer aided VLSI Design
5	Intellectual property rights	Human values & professional ethics
6		VLSI Signal Processing



M.Tech.(Electronics-VLSI) Sem-III

Bharati Vidyapeeth
(Deemed to be University)
College of Engineering, Pune

Elective I- PROGRAMMABLE SYSTEM ON CHIP

TEACHING SCEME

Lectures: 04 Hrs/Week

Practicals:02 Hrs/week

EXAMINATION SCHEME

Duration: 03 Hrs

Theory : 60 Marks

Internal Assessment: 40 Marks

TW&OR:50 Marks

Total Credits: 05

Course prerequisites:
Knowledge of microprocessors and microcontrollers

Course objective:

1. To introduce the students to the Cypress PSoC technology
2. To study the architecture of PSoC
3. To learn interfacing of real world with PSoC

Course Outcomes: Upon Completion of the course, the students will be able to

1. Describe and identify the features of PSoC
2. Design the system for interfacing to the real world.

Contents:

UNIT I (08 hours)

Introduction to PSoC

PSoC Technology, Programmable Routing and Interconnect Configurable Analog and Digital Blocks, CPU Sub System, Families of PSoC (PSoC1, PSoC2, PSoC3,) Difference between PSoC and Conventional MCU.

UNIT II (08 hours)

Introduction to PSoC 3/5

PSoC3/5 architecture-block diagram system wide resources, I/O interfaces, CPU Subsystem, memory organization digital subsystems, analog subsystems

UNIT III (08 hours)

PSoC Design Modules

Cypress PSoC Structure, PSoC Designer Suit, limitations of PSoC improvements of the PSoC, PSoC Subsystem design, PSoC memory management.

UNIT IV (08 hours)

Mixed –Signal Embedded design

Overview of mixed-signal embedded system designs, hardware and software subsystems of mixed-signal architectures, PSoC Hardware components, PSoC software components, PSoC interrupt subsystem, Introduction to PSoC Express, System design using PSoC express**.(8hrs)**

UNIT V (08 hours)

PSoC Components

Universal Digital Blocks (UDB), UDB arrays and digital System Interconnect (DSI),Timer, Counter and PWM,Digital Filter Blocks (DFB),ADC topologies and Circuits Programmable gain amplifiers, Switched capacitor / continuous time, analog routing, flash temperature sensors,DTMF Dialers, Sleep times,UART.12C,SPI,USB,CAN buses.

UNIT VI (08 hours)

System design using PSoC

Interfacing of temperature Sensors and Tachometers, SPI and UART based task communications, Lower Noise Continuous Time Signal Processing with PSoC Data Acquisition and Control System with PSoC, Ultra wide-band RADAR, Serial Bit Receiver with Hardware Manchester Decoder, DTMF Detector, and Ultrasonic Vehicle Parking Assistant, Universal wide-Range Signal Generator.

Text Books:

1. PSoC3, PSoC5 Architecture Technical Reference Manual-Cypress website
2. My First Five PSoC3 Designs (e-book)by Robert Ashby-Cypress website

Reference Books:

1. Designers Guide to the Cypress PSoC by Robert Ashby –Elsevier Publications
2. Introduction to Mixed Signal Embedded Design, Alex Boboli-Springer
3. The Beginners Guide to Using PSoC Express: Mixed –Signal Microcontroller Development Without code by Oliver H.Bailey-Timelines Industries Incorporated,2007
4. PSoC Microcontroller by Fredi Kruger Franzis,2006

Web references

www.cypress.com/go/psoc

www.cypress.com/go/training

www.cypress.com/go/support

www.psocdeveloper.com

Bharati Vidyapeeth
(Deemed to be University)
College of Engineering, Pune

Elective I-NANO ELECTRONICS

TEACHING SCHEME

Lectures: 04 Hrs/Week

Practicals: 02 Hrs/Week

EXAMINATION SCHEME

Duration:03 Hrs

Theory: 60 Marks

Internal Assessment: 40 Marks

TW&OR: 50 Marks

Total Credits: 05

Course Prerequisite:

Physics, Basic electronics

Course Objective:

To learn and understand basic and advance concepts of nanoelectronics.

Course Outcomes: On successful completion of this course, students will be able to

1. Understand basic and advanced concepts of nanoelectronic devices
2. Gain knowledge about Nanostructure devices and logic devices.
3. Know the techniques of fabrication and measurement.

Contents:

UNIT I **(08 hours)**

Basics of nanoelectronics

Capabilities of nanoelectronics – physical fundamentals of nanoelectronics – basics of information theory – the tools for micro and nano fabrication – basics of lithographic techniques for Nanoelectronics

UNIT II **(08 hours)**

Quantum electron devices

classical to quantum physics: upcoming electronic devices – electrons in mesoscopic structure – short channel MOS transistor – split gate transistor – electron wave transistor – electron spin transistor – quantum cellular automate – quantum dot array – Principles of Single Electron Transistor (SET) – SET circuit design – comparison between FET and SET circuit design

UNIT III **(08 hours)**

Fabrication and Measurement Techniques

Growth, fabrication, and measurement techniques for nanostructures- Bulk crystal and heterostructure growth- Nanolithography, etching, and other means for fabrication of nanostructures and nanodevices- Techniques for characterization of nanostructures- Spontaneous formation and ordering of nanostructures- Clusters and nanocrystals- Methods of nanotube growth- Chemical and biological methods for nanoscale fabrication- Fabrication of nano-electromechanical systems

UNIT IV **(08 hours)**

Nanostructure Devices -I

Electron transport in semiconductors and nanostructures- Time and length scales of the electrons in solids- Statistics of the electrons in solids and nanostructures- Density of states of electrons in nanostructures- Electron transport in nanostructures-Electrons in traditional low-dimensional structures- Electrons in quantum wells- Electrons in quantum wires- Electrons in quantum dots

UNIT V **(08 hours)**

Nanostructure devices- II

Resonant-tunneling diodes- Potential-effect transistors- Light-emitting diodes and lasers- Nano-electromechanical system devices- Molecular electronics – elementary circuits – flux quantum devices – application of superconducting devices –Strain –oxide nanowire, Nano designs and Nanocontacts – metallic nanostructures

UNIT VI **(08 hours)**

Logic Devices and Applications

Logic Devices-Silicon MOSFETs-Ferroelectric Field Effect Transistors-Quantum Transport Devices Based on Resonant Tunneling-Single-Electron Devices for Logic Applications-Superconductor Digital Electronics-Quantum Computing Using Superconductors-Carbon Nanotubes for Data Processing- Molecular Electronics

Text Books :

1. Karl Goser, Peter Glösekötter, Jan Dienstuhl,“Nanoelectronics and Nanosystems: From Transistors to Molecular and Quantum Devices“, Springer 2004

2. Mick Wilson, Kamali Kannangara, Geoff Smith, Michelle Simmons, Burkhard Raguse,”Nanotechnology: basic science and emerging technologies”, Overseas Press (2005)

Reference Books:

1. Rainer Waser (edition, 2005) ,”Nanoelectronics and Information Technology” ,John Wiley & Sons, Germany.

2. Vladimir V. Mitin, Viatcheslav A. Kochelap, Michael A. Stroscio, “Introduction to Nanoelectronics: Science, Nanotechnology, Engineering, and Applications”, Cambridge University Press 2011

3. Supriyo Datta,“Lessons from Nanoelectronics: A New Perspective on Transport”, World Scientific 2012 6. George W. Hanson,“Fundamentals of Nanoelectronics”, Pearson 2009

4. Korkin, Anatoli; Rosei, Federico (Eds.), “Nanoelectronics and Photonics”,Springer 2008

5. Mircea Dragoman, Daniela Dragoman, “Nanoelectronics: principles and devices”, CRC Press 2006

6. W. R. Fahrner, Nanotechnology and Nan electronics: Materials, Devices, Measurement Techniques (SpringerVerlag Berlin Heidelberg 2005)

7. Mark A. Reed, Takhee Lee,“Molecular nanoelectronics”, American Scientific Publishers 2003

8.. Jaap Hoekstra, “Introduction to Nanoelectronic Single-Electron Circuit Design”, Pan Stanford Publishing 2010

Elective I- ADVANCED DIGITAL SYSTEM DESIGN

TEACHING SCHEME	EXAMINATION SCHEME
Lectures: 04 Hrs/Week	Duration:03 Hrs
Practicals: 02 Hrs/Week	Theory: 60 Marks
	Internal Assessment: 40 Marks
	TW&OR: 50 Marks
	Total Credits: 05

Course Prerequisite:

VLSI Design Technology , Hardware Description Language

Course Objective:

- To understand theory and to learn design of digital system.
- Learn about design and simulation of digital circuits using VHDL/Verilog

---

Course Outcomes: On successful completion of this course, students will be able to

1. Design the sequential circuits
2. Understand advanced design of Synchornos and Asynchornous circuits
3. Ability to conceptualize FSM.
4. Ability to apply concepts of PLD designs.
5. Ability to system design using VHDL.
6. Understanding logic and system design using Verilog.

Contents:

UNIT I **(08 hours)**

Sequential Circuit Design

Analysis of clocked synchronous sequential circuits and modeling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits, design of iterative circuits-ASM chart and realization using ASM

UNIT II **(08 hours)**

Asynchronous Sequential Circuit Design

Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment-transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller

UNIT III **(08 hours)**

FSM Design using Verilog/VHDL

Mealy and Moore designs, Implementation, Moore architecture and Verilog/VHDL templates,Mealy architecture and Verilog/VHDL templates.

UNIT IV **(08 hours)**

Synchronous Design using Programmable Devices

Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL – Realization of finite state machine using PLD – FPGA – Xilinx FPGA, coding for FPGAs. Designing with FPGAs: Design flow for FPGAs,prototyping with FPGAs, and debugging.

UNIT V **(08 hours)**

System Design using VHDL

VHDL operators–Arrays – concurrent and sequential statements – packages- Data flow–Behavioral – structural modeling – compilation and simulation of VHDL code–Test bench - Realization of combinational and sequential circuits using HDL – Registers – counters – sequential machine – serial adder –Multiplier- Divider – Design of simple micropr ocessor

UNIT VI **(08 hours)**

Logic and System Design Using Verilog

Logic design with Verilog: logic design with behavioral models of combinational and sequential logic, synthesis of combinational and sequential logic, design and synthesis of data path controllers, programmable logic and storage devices, algorithms and architectures for digital processors, architectures for arithmetic processors

Text Books :

1. Charles H.Roth Jr “Fundamentals of Logic Design” Thomson Learning 2004.

2. Nripendra N Biswas “Logic Design Theory” Prentice Hall of India,2001

3. Douglas L.Perry “VHDL programming by Example” Tata McGraw.Hill – 2006.

Reference Books:

1. Parag K.Lala “Fault Tolerant and Fault Testable Hardware Design” B S Publications,2002

2. Parag K.Lala “Digital system Design using PLD” B S Publications,2003.

3. Charles H Roth Jr.”Digital System Design using VHDL” Thomson learning, 2004

4. Michael D.Ciletti “ Advanced Digital Design with the Verilog HDL (2nd Edition 2017)”, ISBN: 9789332584464, Publisher: Pearson.

Bharati Vidyapeeth
(Deemed to be University)
College of Engineering, Pune

Elective I-ALGORITHMS FOR VLSI DESIGN AUTOMATION

TEACHING SCEME

Lectures: 04 Hrs/Week

Practicals: 02 Hrs/Week

EXAMINATION SCHEME

Duration: 03 Hrs

Theory : 60 Marks

Internal Assessment: 40 Marks

TW&OR:50 Marks

Total Credits: 05

Course Prerequisites:

Analog and Digital VLSI Design, Engineering Mathematics

Course objective:

To introduce the student to the algorithms used for VLSI Design Automation

---

Course Outcomes: After successfully completing the course students will be able to

1. Apply various algorithms for VLSI design.
2. Conceptualize placement, floorplanning and pin assignment.
3. Plan global and detailed routing.
4. Apply concepts of via minimization and compaction

Contents:

UNIT I (08 Hours)

Basic Algorithms
Basic Terminology, Complexity issues, NP- hardness, Graph algorithms, Computational geometry algorithms.

UNIT II (08 Hours)
Partitioning
Problem formulation, Classification of partitioning algorithms, Group migration algorithms, Simulated annealing & evolution, Other partitioning algorithms.

UNIT III (08 Hours)

Placement, Floor Planning and Pin Assignment
Problem formulation, Classification of Placement algorithms, Overview of placement algorithms, Constrain based floor planning, Floor planning algorithms for mixed block and cell design, General and channel pin assignment.

UNIT IV (08 Hours)

Global Routing
Problem formulation, classification of global routing algorithms, Maze routing algorithms, Line probe algorithm, Steiner tree based algorithms, ILP based approaches.

UNIT V (08 Hours)

Detailed Routing
Problem formulation, classification of routing algorithms, single layer routing algorithms, Two layer channel routing algorithm, Three layer channel routing algorithm & switch box routing algorithms.

UNIT VI (08 Hours)

Over The Cell Routing & Via Minimization:

Two layers over the cell routers, Constrained & unconstrained via minimization.

Compaction:

Problem formulation, one-dimensional compaction, Two dimension based compaction, hierarchical compaction.

Text Books/ References:

1. Naveed Shervani, ,"Algorithms for VLSI physical design Automation", Kluwer Academic Publisher, Third edition, 1999.
2. Christophn Meinel & Thorsten Theobold, "Algorithm and Data Structures for VLSI Design", Springer, 1998.
3. Rolf Drechsheler ,"Evolutionary Algorithm for VLSI", Second edition KAP, 1998
4. Trimburger, ,"Introduction to CAD for VLSI", Kluwer Academic publisher, 2002

Bharati Vidyapeeth
(Deemed to be University)
College of Engineering, Pune

Elective II -ASIC DESIGN

TEACHING SCEME

Lectures: 04 Hrs/Week

Practicals: 02 Hrs/Week

EXAMINATION SCHEME

Duration: 03 Hrs

Theory : 60 Marks

Internal Assessment: 40 Marks

Total Credits: 05

Course prerequisites:

Digital VLSI Design

Course objective:

The course focuses on the semi custom IC Design and introduces the principles of design logic cells, I/O cells and interconnects architecture, with equal importance given to FPGA and ASIC styles.

Course Outcomes: On successful completion of this course, students will be able to

1. Apply fundamentals of ASIC and its design methods
2. Understand block level abstractions of FPGA and ASIC design
3. Gain knowledge on programmable architectures for ASICs
4. Conceptualize the physical design of ASIC.

Contents:

UNIT-I (08 Hours)

Introduction to ASICS, CMOS Logic and ASIC Library Design
Types of ASICs, Design flow, Combinational Logic Cell, Sequential logic cell, Data path logic cell, Transistors as Resistors, Transistor Parasitic Capacitance, Logical effort.

UNIT-II (08 Hours)

Programmable ASICS, Programmable ASICS Logic Cells and Programmable ASICS I/O Cells
Anti fuse, static RAM , EPROM and EEPROM technology, Actel ACT , Xilinx LCA, Altera FLEX , Altera MAX DC & AC inputs and outputs , Clock & Power inputs, Xilinx I/O blocks.

UNIT-III (08 Hours)

Programmable ASIC Logic Cells
Actel ACT, Xilinx LCA , Xilinx EPLD, Altera MAX 50 00 and 7000 , Altera MAX 9000 , Altera FLEX, Design systems, Logic Synthesis , Half gate ASIC, Schematic entry, Low level design language.

UNIT-IV (08 Hours)

Logic Synthesis, Simulation and Testing
VHDL and logic synthesis, Types of simulation, Boundary scan test, Fault simulation, Automatic test pattern generation.

UNIT-V (08 Hours)

ASIC Floor Planning, Placement and Routing
System partition, FPGA partitioning, Partitioning methods, Floor planning, Placement, Physical design flow, Global routing, Detailed routing

UNIT-VI (08 Hours)

Optimization Algorithms

Planar subset problem(PSP), single layer global routing single layer detailed routing wire length and bend minimization technique, over the cell(OTC) Routing, multichip modules(MCM), Programmable logic arrays, Transistor chaining, Weinberger Arrays, Gate Matrix Layout.

Reference Books:

1. M.J.S.Smith, " Application Specific Integrated Circuits", Pearson,2003
2. Steve Kilts, “Advanced FPGA Design,” Wiley Inter-Science.
3. Roger Woods, John McAllister, Dr. Ying Yi, Gaye Lightbod , “FPGA based Implementation of Signal Processing Systems”, Wiley, 2008
4. Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing ", Mc Graw Hill, 1994.
5. Douglas J. Smith, HDL Chip Design , Madison, AL, USA: Doone Publications, 1996.
6. Jose E. France, Yannis Tsividis, "Design of Analog Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994
7. Farzad Nekoogar and Faranak Nekoogar, “From ASICs to SOCs: A Practical Approach”, Prentice Hall PTR, 2003.

Bharati Vidyapeeth
(Deemed to be University)
College of Engineering, Pune

Elective II -TESTING AND VERIFICATION OF VLSI DESIGN

TEACHING SCEME	EXAMINATION SCHEME
Lectures: 04 Hrs/Week	Duration: 03 Hrs
Practicals: 02 Hrs/Week	Theory : 60 Marks
	Internal Assessment: 40 Marks
	TW&OR:50 Marks
	Total Credits: 05

Course prerequisites:

Analog and Digital VLSI Design

Course objective:

To introduce the student to the mathematical and scientific principles based on which systematic test and validation can be carried out on multimillion transistor VLSI design.

Course Outcomes: On successful completion of this course, students will be able to

1. Apply various fault modeling for digital circuits.
2. Test VLSI circuits.
3. Conceptualize Verification process.
4. Plan verification using verification tools.
5. Apply concepts of DFT and BIST.

Contents:

UNIT I (08 Hours)

Introduction to Verification

Importance of verification, Testbench, Human factor, What is being verified, Functional verification approaches, Testing v/s Verification, Verification and design reuse, Cost of verification.

UNIT II (08 Hours)

Verification Tools

Linting Tools, Simulators, Third party models, Waveform viewers, Code coverage.

UNIT III (08 Hours)

Verification Plan

Role of verification plan, Levels of verification, Verification strategies, From specification to features, From features to testcases, From testcases to testbenchs.

UNIT IV (08 Hours)

Basics of Testing and Fault Modeling

Introduction to Testing, Faults in digital circuits, Modeling of faults, Logical Fault Models, Fault
Detection, Fault dominance, Delay fault models.

UNIT V (08 Hours)

Test Generation for Combinational and Sequential Circuits

Test generation for combinational logic circuits, Testable combinational logic circuit design, Test generation for sequential circuits, Design of testable sequential circuits.

UNIT VI (08 Hours)

DFT and BIST

Design for Testability, Ad-hoc design, Scan based design, Built-In-Self-Test.

Text Books/ References:

1. Janick Bergeron ,"Writing Testbenches: Functional Verification of HDL Models", Springer, Second Edition, 2003
2. M.L. Bushnell and V.D. Agrawa,"Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits- l, "Kluwer Academic Publishers, 2002
3. A.L.Crouch ,"Design Test for Digital IC's and Embedded Core Systems", Prentice Hall International, 2002.
4. M.Abramovici, M.A.Breuer and A.D. Friedman ,"Digital systems and Testable Design", Jaico Publishing House, 2002.

Bharati Vidyapeeth
(Deemed to be University)
College of Engineering, Pune

Elective II-ARTIFICIAL NEURAL NETWORK

TEACHING SCEME	**EXAMINATION SCHEME**
Lectures: 04 Hrs/Week	Duration: 03 Hrs
Practicals: 02 Hrs/Week	Theory : 60 Marks
	Internal Assessment: 40 Marks
	TW&OR:50 Marks
	Total Credits: 05

Course prerequisites:

- Basic knowledge of human nervous systems.
- Basic knowledge of mathematical concepts like state-space, Matrix fundamentals.

Course objective:

This course provides in depth knowledge of Artificial Neural Network and role of ANN in different application areas.

Course Outcomes: On successful completion of this course, students will be able to

1 Identify potential use of learning approaches of ANN.
2. Analyze role of perceptron, Adaline & Madeline networks
3. Evaluate different application scenarios of ANN

Contents:

UNIT I (08 Hours)

Introduction and ANN Structure.
Biological neurons and artificial neurons, Model of an ANN, ANN Terminologies, Activation functions used in ANNs, Typical classes of network architectures, Mc-Culloch-Pitts Neuron Model, Learning rules.

UNIT II (08 Hours)

Mathematical Foundations and Learning mechanisms.
Re-visiting vector and matrix algebra, State-space concepts, Concepts of optimization, Error-correction learning, Memory-based learning, Hebbian learning, Competitive learning.

UNIT III (08 Hours)

Single layer perceptrons. Adaline & Madeline Networks
Structure and learning of perceptrons, Pattern classifier - introduction and Bayes' Classifiers, Perceptron as a pattern classifier, Perceptron convergence, Limitations of a perceptrons, Adaline architecture, algorithm, MR-I, MR-II algorithms.

UNIT IV (08 Hours)

Feedforward ANN.
Structures of Multi-layer feedforward networks, Back propagation algorithm, Back propagation - training and convergence, Functional approximation with back propagation, Practical and design issues of back propagation learning. Radial Basis Function Networks, Pattern separability and interpolation, Regularization Theory, Regularization and RBF networks, RBF network design and training, Approximation properties of RBF.

UNIT V (08 Hours)

Competitive Learning and Self organizing ANN

General clustering procedures, Learning Vector Quantization (LVQ), Competitive learning algorithms and architectures, Self organizing feature map, Properties of feature maps, Mexican Net, Hamming Net.

UNIT VI (08 Hours)

Special Networks & Applications of Neural Networks

Support Vector machines**,** Design of an SVM, Examples of SVM, Probabilistic Neural Network, Boltzmann Machine with learning, cognitron, simulated annealing, applications of Neural Networks in bioinformatics, forecasting, healthcare, robotics, pattern recognition.

Text Books/ References:

- Simon Haykin, "Neural Networks: A comprehensive foundation", Second Edition, Pearson Education Asia.
- Satish Kumar, "Neural Networks: A classroom approach", Tata McGraw Hill, 2004.
- Robert J. Schalkoff, "Artificial Neural Networks", McGraw-Hill International Editions, 1997.
- S.N. Sivananadam, "Introduction to Neural Networks using MATLAB", The McGraw-Hill, 2006.

Bharati Vidyapeeth
(Deemed to be University)
College of Engineering, Pune

Self Study Paper I -LOW POWER VLSI DESIGN

TEACHING SCEME

Lectures: 04 Hrs/Week

EXAMINATION SCHEME

Duration: 03 Hrs

Theory : 60 Marks

Internal Assessment: 40 Marks

Total Credits: 04

Course prerequisites:

Analog and Digital VLSI Design

Course objective:

To introduce the student to the concept of low power VLSI design, power estimation and power optimization

---

Course Outcomes:

1. Ability to apply various low power techniques at device and circuit level.
1. Ability to design low power VLSI circuits.
2. Ability to conceptualize low power VLSI basics.
3. Ability to plan low power architectures.
4. Ability to apply concepts of low power design at system level.

Contents:

UNIT I (08 Hours)

Low Power Basics

Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits, Emerging Low power approaches, Physics of power dissipation in CMOS devices.

UNIT II (08 Hours)

Impact of Device & Technology on Low Power

Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

UNIT III (08 Hours)

Low Power Design

Circuit level:
Power consumption in circuits, Flip Flops & Latches design, High capacitance nodes, Low power digital cells library

Logic level:
Gate Reorganization, Signal Gating, Logic Encoding, State Machine Encoding, Pre-Computation Logic

UNIT IV (08 Hours)

Low power Architecture & Systems

Power & performance management, Switching activity reduction, Parallel and Pipeline architecture for low power memory design.

UNIT V (08 Hours)

Low power Clock Distribution

Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co-design of clock network

UNIT VI (08 Hours)

Algorithm & architectural level methodologies

Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation &
synthesis.

Text Books/ References:

1. Gary K. Yeap ,"Practical Low Power Digital VLSI Design", KAP, 2002
2. Rabaey, Pedram ,"Low power design methodologies", Kluwer Academic, 1997
3. Kaushik Roy, Sharat Prasad ,"Low-Power CMOS VLSI Circuit Design",Wiley,2000

Bharati Vidyapeeth
(Deemed to be University)
College of Engineering, Pune

Self Study Paper I -IC FABRICATION TECHNOLOGY

TEACHING SCHEME

Lectures: 04 Hrs/Week

EXAMINATION SCHEME

Duration: 03 Hrs

Theory : 60 Marks

Internal Assessment: 40 Marks

Total Credits: 04

Course prerequisites:

Physics, Chemistry

Course objective:

To understand theory and to learn IC Fabrication Technology..

Course Outcomes: On successful completion of this course, students will be able to

1. Conceptualize steps required for IC fabrication.
2. Apply concepts of Oxidation, Lithography , Chemical Vapour Deposition and Metal Film Deposition.

Contents:

UNIT-I (08 Hours)

Environment for VLSI Technology
Basic Fabrication Steps, Concepts of Clean room and safety requirements, Wafer cleaning processes and Wet chemical etching techniques.

UNIT-II (08 Hours)

Oxidation
Kinetics of Silicon dioxide growth for thick, thin and ultrathin films. Oxidation technologies in VLSI and ULSI, High k and Low k dielectrics

UNIT-III (08 Hours)

Lithography
Photolithography, E-beam lithography and newer lithography techniques for VLSI/ULSI.

UNIT-IV (08 Hours)

Chemical Vapour Deposition Techniques
CVD techniques for deposition of polysilicon, silicon dioxide, silicon nitride and metal film

UNIT-V (08 Hours)

Metal Film Deposition
Evaporation and sputtering techniques, Failure mechanisms in metal interconnects Multi-level metallization schemes

UNIT-VI (08 Hours)

Rapid Thermal Processing
PECVD, Plasma etching and RIE techniques; RTP techniques for annealing, growth and deposition of various films for use in ULSI

Reference Books:

1. S.K. Ghandhi, "VLSI Fabrication Principles," John Wiley Inc., New York, 1994(2nd Edition).
2.S.M. Sze (Ed), "VLSI Technology", 2nd Edition, McGraw Hill, 1988.

3.Plummer, Deal , Griffin “Silicon VLSI Technology: Fundamentals, Practice & Modeling” PH,2001.
4.P. VanZant , “Microchip Fabrication”, 5th Edition, MH , 2000.

Bharati Vidyapeeth
(Deemed to be University)
College of Engineering, Pune

Self Study Paper I -IN-VEHICLE NETWORKING

TEACHING SCEME

Lectures: 04 Hrs/Week

EXAMINATION SCHEME

Duration: 03 Hrs

Theory: 60 Marks

Internal Assessment: 40 Marks

Total Credits: 04

Course prerequisites:

Knowledge of Basic Electronics and Physics

Course objective:

1. To Provide Students with a working of in-vehicle network systems and exposure to aspects of design, development, application issues associated with those systems.

2. To Provide Knowledge in concepts of capture of Sensor data, Storge and exchange of data to obtain remote services.

Course Outcomes: On successful completion of this course, students will be able to

1. Get knowledge in Information –intensive applications that are being enabled for vehicles by a combination of telecommunication computing technology.
2. Develop communications, and navigation/in automotive telemetries.

Contents:

UNIT I (08 hours)

Basics of In-vehicle Networking

Over view of Data communication and networking –need for In-Vehicle networking-layers of OSI reference model –multiplexing and de-multiplexing concepts-vehicles

UNIT II (08 hours)

Networks and Protocols

Over view of general purpose networks and protocols –Ethernet, TCP, UDP, IP, ICMP, ARM, RARP, Over view CAN-Fundamentals-selecting CAN controller-CAN development tools-CAN application areas.

CAN protocol: principles of Data exchange –real time transmission –message frame formats, bit encoding bit physical layer standards

UNIT III (08 hours)

CAN Higher Layer Protocol

Introduction to CAN open-Device net –TTCAN-SAE J1939-overview of CAN open and application in transportation electronics –CAN open standards

UNIT IV (08 hours)

LIN Protocol

LIN standard over view – applications- LIN communication concept message frame-development flow

UNIT V (08 hours)

MOST and Flex Ray

MOST over view –Data rates –data types-topology –application areas –Flex Ray Introduction-network topology –ECUs and bus interfaces –controller host interface and protocol operation controls-media Access Control and frame and Symbol processing –Coding/decoding unit-Flex Ray Scheduling –message processing –wakeup/Startup-applications

UNIT VI (08 hours)

Wireless Systems

Introduction to wireless system –GPS –Setting receivers-Positioning-activating the navigation function –Concept of latitude and grid System-mapping and location technologies-Application.

Reference Books:

1. B.Hoffman-Wellenhof,H.Lichtenegger and J.Collins,"GPS Theory and practice ".4th revised edition, Spriger,Wein New York,1997
2. A.Leick,"GPS satellite Surveying",2edition,John Wiley and Sons, New York, 1995
3. Wireless Systems,W.C.Y.lee,prentice hall Publ. (LBS) -mobile and Wireless design
4. Konrad Etschberger, Controller Area Network, IXXAT Automation August 22, 2001.
5. Olaf Pfeiffer, Andrew Ayre,Christian Keydel,Embedded Networking with CAN and CAN open ,Anna books/Rtc Books,Novenber 1,2003
6. Ronald K Jurgen, Automotive Electronics Handbook, McGraw-Hill Lnc.1999.
7. Dennis Foy,Automotive Telemetric ,Red Hat,2002.

Bharati Vidyapeeth
(Deemed to be University)
College of Engineering, Pune

Self Study Paper I -RESEARCH METHODOLOGY

TEACHING SCHEME

Lectures: 04 Hrs/Week

EXAMINATION SCHEME

Duration: 03 Hrs

Theory: 60 Marks

Internal Assessment: 40 Marks

TW & OR : 50 Marks

Total Credits: 04

Course prerequisites:

- Basic knowledge of modeling and simulation.
- Basic knowledge of probability and statistics

Course objective:

This course provides basic knowledge of Research Methodology in different areas.

Course Outcomes: On successful completion of this course, students will be able to

1. Learn research fundamentals like objectives, literature review process.
2. Apply the various methods of modeling and simulation.
3. Apply the probability statistics in the simulation.
4. Write the technical research paper with required presentation.
5. Know about of Information communication technology: e-research, indices, patents, virtual lab etc

Contents:

UNIT I (08 Hours)

Research fundamentals

Definition, objectives, motivation, types of research and approaches, research- descriptive, conceptual, theoretical, applied and experimental

UNIT II (08 Hours)

The initial research process

Literature review, research design, assortment of the problem, identification of problem, defining a problem, objective, sub objective and scope, assumptions, validation criteria, research proposal(synopsis)

UNIT III (08 Hours)

Mathematical modeling and simulation

Mathematical modeling – need, techniques and classification, system models –types, static, dynamic, system simulation – why to simulate, technique of simulation, Monte Carlo simulation, types, continuous modeling, discrete model

UNIT IV (08 Hours)

Probability and statistics in simulation

Role of probability and statistics in simulation, statistical distributions, inference about the difference in means, statistical output analysis

UNIT V (08 Hours)

Design of experiment

Strategy of experimentation, types, basic principle, guidelines, need of precision, types of errors

UNIT VI (08Hours)

Report writing and presentation of results

Need, report structure, formulation, sections, protocols, graphs, tables, IEEE format, evaluation of report, writing abstract, writing technical paper, Introduction of Information communication technology: e-research, indices, patents, virtual lab, digital lab, ethical issues in research

Reference books:

1. Yogesh Kumar Sing ,"Fundamental of Research Methodology and Statistics" , New Age International Publishers
2. C.R. Kothari, "Research Methodology: Methods and Techniques," New Age International Publishers, 2nd revised Edition
3. Deepak Chawla, Neena Sondhi ,"Research Methodology, Concepts and Cases" , Vikas Publishing House Pvt. Ltd
4. Hamdy A. Taha ,"Simulation Modeling and Simnet" , Prentice Hall International Edition
5. Geoffrey Gorden ,"System Simulation" , Prentice Hall of India Pvt. Ltd.
6. J N Kapur ,"Mathematical Modeling" , Wiley Eastern Ltd
7. Douglas C. Montgomery ,"Design and analysis of Experiments" , Wiley Student Edition, 7th Edition
8. Capt. Dr.Nitin P. Soaje ,"Role of ICT in Doctoral Research "

Bharati Vidyapeeth
(Deemed to be University)
College of Engineering, Pune

Self Study Paper I -INTELLECTUAL PROPERTY RIGHTS

TEACHING SCHEME

Lectures: 04 Hrs/Week

EXAMINATION SCHEME

Duration: 03 Hrs

Theory : 60 Marks

Internal Assessment: 40 Marks

TW & OR: 50 Marks

Total Credits: 04

Course objective:

- To introduce fundamental aspects of intellectual property rights to students.
- To provide case studies to demonstrate the application of legal concepts in engineering.

Course Outcomes: On successful completion of this course, students will be able to

- Understand the international intellectual property rights system.
- Use the necessary analytical tools to understand intellectual property in its broader environment

---

Contents:

UNIT I (08 Hours)

Overview of Intellectual Property

Introduction and need for Intellectual Property Rights (IPR),Different categories of IP in instruments, Rational behind Intellectual Property, Rights of the owner of the IP. IPR in India-Genesis & development, International Background of Intellectual Property, some important examples of IPR.

UNIT II (08 Hours)

Patents

Introduction to patents, Concept: Novelty, Utility, Patent document, Granting of patent, Rights of a patent, Drafting of a patent, Filling of a patent, The Indian Patent law,Infringement

UNIT III (08 Hours)

Copyright

Introduction to Copyright, Originality, Works protected under Copyright Law, Authorship and Ownership

UNIT IV (08 Hours)

Trademarks

Introduction, Rights of trademark, Need for protection of trademarks, Types of trademarks, Registration of trademarks, Rights of Registered Trademark Owners, Infringement of trademarks

UNIT V (08 Hours)

Acquisition & maintenance of Intellectual Property Rights

Introduction to Acquisition & maintenance of Intellectual Property Rights,Intellectual property offices(IPOs),Costs-Patents,costs-Trademark,Costs-Copyright

UNIT VI (08 Hours)

Enforcement of Intellectual Property Rights

Introduction to Enforcement of Intellectual Property and Global economy. The knowledge of economy & IP, valuation & accounting of Intangible assets, Management of IP in knowledge economy.

Text books/Reference

1) W.R. Cornish, 'Intellectual Property', Sweet & Maxwell, London (2000)

2) N.S. Gopalakrishnan & T.G. Agitha, 'Principles of Intellectual Property' Eastern Book Company, Lucknow.

3) P. Narayana, 'Patent Law', Wadhwa Publication.

4) V. V. Sopale, 'Managing Intellectual Property: The Strategic Importance', Second edition, PHI.

M.Tech.(Electronics-VLSI) Sem-IV

Bharati Vidyapeeth
(Deemed to be University)
College of Engineering, Pune

Self Study Paper II- GENETIC ALGORITHMS FOR VLSI DESIGN

TEACHING SCEME	EXAMINATION SCHEME
Lectures: 04 Hrs/Week	Duration: 03 Hrs
	Theory: 60 Marks
	Internal Assessment: 40 Marks
	TW & OR: 50 Marks
	Total Credits: 04

Course prerequisites:

Analog and Digital VLSI Design

Course objective:

To introduce the student to the concept of Genetic Algorithm for VLSI

Course Outcomes:

1. Ability to apply Genetic Algorithm for VLSI Design.
2. Ability to optimize VLSI Design through algorithm.
3. Ability to conceptualize VLSI design flow through Genetic Algorithm .

Contents:

UNIT I (8 hours)

VLSI Design

Design Methodology and Hardware Implementation Methodologies, Digital ASIC Implementation

UNIT II (8 hours)

Genetic Algorithms

Components of a GA Based Optimization Engine, Individual Encoding, Fitness of an Individual, Selection Mechanism Genetic Operators, Crossover Operators, Uniform Crossover, Elitism in Genetic Algorithms, Multi-Objective Genetic Algorithms

UNIT III (8 hours)

Multi-Objective Genetic Floorplanning For Vlsi Asics

Multi-objective Optimization, Floor planning and Floor planning Using Sequence Pair Representation, Conversion from a Floor plan to a Sequence Pair, Conversion from a Sequence Pair to a Floor plan

UNIT IV (8 hours)

FPGA Based Genetic Algorithm

Pseudo-Random Number Generation and GA Performance, Basics of Evolvable Hardware, FPGA Based Genetic Algorithm, Implementation and Interfacing, Design Considerations for ASIC Implementation, RT-Level Simulations, Runtime Comparison of Implemented design.

UNIT V (8 hours)

Power Estimation

Application of GA-Standard cell placement-GA for ATG-problem encoding- fitness function-GA vs Conventional algorithm

UNIT VI (8 hours)

Hybrid Genetic

Genetic encoding-local improvement-WDFR-Comparison of Cas-Standard cell placement-GASP algorithm-unified algorithm.

Text Books

1. Pinaki Mazumder,E.MRudnick,"Genetic Algorithm for VLSI Design,Layout and test

Automation", Prentice Hall,1998.

References :

1. Randy L. Haupt, Sue Ellen Haupt, "Practical Genetic Algorithms" Wiley – Interscience,1977.

2. Ricardo Sal Zebulum, Macro Aurelio Pacheco, Marley Maria B.R. Vellasco, Marley Maria Bernard Vellasco "Evolution Electronics: Automatic Design of electronic Circuits and Systems Genetic Algorithms", CRC press, 1st Edition Dec 2001.

3. John R.Koza, Forrest H.Bennett III, David Andre , Morgan Kufmann, "Genetic Programming Automatic programming and Automatic Circuit Synthesis", 1st Edition , May 1999.

Bharati Vidyapeeth
(Deemed to be University)
College of Engineering, Pune

Self-Study Paper II: FUZZY LOGIC SYSTEMS

TEACHING SCHEME

Lectures: 04 Hrs/Week

EXAMINATION SCHEME

Duration: 03 Hrs

Theory: 60 Marks

Internal Assessment: 40 Marks

Total Credits: 04

Course prerequisites:

- Basic knowledge of set & probability theory.
- Basic knowledge of prepositional logic & control systems

Course objective:

This course provides in depth knowledge of Fuzzy Logic and role of Fuzzy Logic systems in different application areas.

Course Outcomes: On successful completion of this course, students will be able to

1. Analyze basic concepts of fuzzy sets, fuzzy relation and fuzzy arithmetic.
2. Identify potential use of fuzzy logic controller in different applications.
3. Evaluate fuzzy logic systems with fuzzy classification, fuzzy pattern recognition and hybrid systems.

Contents:

UNIT I (08 Hours)

Classical Sets and Fuzzy Sets

Crisp Sets: An Overview, Fuzzy Sets: Basic Types, Fuzzy Sets: Basic Concepts, Characteristics and Significance of the Paradigm Shift, Additional Properties of alpha Cuts, representations of Fuzzy Sets, Extension Principle for Fuzzy Sets, Types of Operations, Fuzzy complements, Fuzzy Intersections: t-Norms, Fuzzy Unions: t-Conorms, Multivalued Logic, Fuzzy Propositions, Fuzzy Quantifiers.

UNIT II (08 Hours)

Classical Relations and Fuzzy Relations

Cartesian Product ,crisp relations, operations on crisp Relations, properties of crisp relations, composition, Fuzzy Relations, operations on fuzzy relations, properties of fuzzy relations, Fuzzy Tolerance and Equivalence Relations, Fuzzy Compatibility Relations, Fuzzy Ordering Relations.

UNIT III (08 Hours)

Fuzzy Arithmetic, Fuzzification and Defuzzification

Fuzzy Numbers, Linguistic Variables, Arithmetic Operations on intervals, Arithmetic Operations on Fuzzy Numbers, Lattice of Fuzzy Numbers, Fuzzy Equations, Fuzzification, Defuzzification to Crisp Sets, λ-Cuts for Fuzzy Relations, Defuzzification to Scalars.

UNIT IV (08 Hours)

Fuzzy Systems

Conventional Control Systems, Analysis, Design, PID Control, Fuzzy Logic Controller (FLC), Design, Defuzzification, Analysis, Simplified Examples of Applications- Washing machine, Vacuum cleaner. Fuzzy Control System Design, Aircraft Landing Control Problem, Fuzzy Engineering Process Control, Fuzzy Statistical Process Control. Fuzzy Neural Networks, Fuzzy Automata.

UNIT V (08 Hours)

Fuzzy Classification & Fuzzy Pattern Recognition

Classification by Equivalence Relations, Cluster Analysis, Cluster Validity, *c*-Means Clustering, Hard *c*-Means (HCM), Fuzzy *c*-Means (FCM), Fuzzy *c*-Means Algorithm, Classification Metric, Hardening the Fuzzy *c*-Partition, Similarity Relations from Clustering, Feature Analysis, Partitions of the Feature Space, Single-Sample Identification, Multifeature Pattern Recognition.

UNIT VI (08 Hours)

Hybrid Systems & Applications of Fuzzy Logic

Hybrid Systems, Fuzzy Neuron, Multilayer FNN Architectures, Fuzzy ART, Fuzzy ARTMAP Neural Fuzzy Systems, economics application, civil & industrial applications, Fuzzy Systems and Genetic Algorithms, Fuzzy Regression, Interpersonal Communication.

Text Books/ References:

1. Timothy Ross, “Fuzzy Logic with Engineering Applications", Third Edition, Wiley publication.
2. George J. Klir & Bo Yuan, “Fuzzy Sets & Fuzzy Logic Theory & Applications”, Prentice Hall India, 2007.
3. Ahmad M. Ibrahim “Fuzzy Logic for Embedded Systems Applications” 2003, Elsevier Science.

Bharati Vidyapeeth
(Deemed to be University)
College of Engineering, Pune

Self-Study Paper II: BIOMEDICAL INSTRUMENTATION

TEACHING SCHEME

Lectures: 04 Hrs/Week

EXAMINATION SCHEME

Duration: 03 Hrs
Theory: 60 Marks
Internal Assessment: 40 Marks
Total Credits: 04

Course prerequisites:

- Knowledge of basic cell structure, organs and systems in the human body

---

Course objective:

1. To make student understand different body systems.
2. To introduce amplifiers in order to design ECG Preamplifier system to pick up ECG waveform from the body.
3. To introduce various types of blood pressure monitoring and pulse oxymetry techniques.
4. To make student understand the importance of respiratory organs and parameters.
5. To make student understand various types of clinical lab equipments and its applications.
6. To introduce importance of electrosurgical equipment and electrodes used for electrosurgical

---

Course Outcomes: On successful completion of this course, students will be able to

1. Classify different body systems with their functions.
2. Design ECG preamplifier system to pick up ECG waveform from the body.

3. Categorize various pressure transducers as well as measurement techniques used for blood pressure monitoring.
4. Describe respiratory system organs, parameters and respiratory transducers.
5. Describe clinical equipments used in the pathology lab for blood test and analysis.
6. Classify various electrodes and techniques used for surgery.

Contents

UNIT I (08 hours)

Human Body System

Human body as a uniquely adaptable organism , Overview of Different systems

UNIT II (08 hours)

Amplifier Systems for ECG

Introduction to amplifiers in biomedical electronics,ECG wave form,Standard lead system,ECG Preamplifier.

UNIT III (08 hours)

Blood Pressure and Blood Flow Measurements

Physiological pressures, Blood pressure measurements, Pressure transducers, pulse oximetry

UNIT IV (08 hours)

Respiratory System Measurements

Introduction to human respiratory system,organs of Respiration,Parameters of respiration,Respiratory transducers, plethysmography.

UNIT V (08 hours)

Clinical Laboratory Equipments

Blood components, overview of Laboratory measurements,Blood gas Analyzer,Blood cell counters,Spectrophotometer,Blood Tests and analyzers.

UNIT VI (08 hours)

Electrosurgical Equipments

Introduction to Electrosurgical Unit ,electro surgery circuits, Electro surgery safety, Patients safety

Text Books:

1.Joseph.J.Carr and John.M.Brown, "Introduction to Biomedical Equipment Technology",Pearson Education.

References:

1.Arthur C Guyton, “Medical Physiology”, Prism Book.

2.Leslie Cromwell,Fred.J.Weibel,”Biomedical Instrumentation and Measurements”, PHI.

Bharati Vidyapeeth
(Deemed to be University)
College of Engineering, Pune

Self-Study Paper II: COMPUTER AIDED VLSI DESIGN

TEACHING SCHEME

Lectures: 04 Hrs/Week

EXAMINATION SCHEME

Duration: 03 Hrs

Theory: 60 Marks

Internal Assessment: 40 Marks

Total Credits: 04

Course prerequisites:

VLSI Design

Course objective:

The course will introduce CAD tools required for VLSI.

Course Outcomes:

On successful completion of this course, students will effectively utilize various CAD tools for VLSI design.

Contents

UNIT I
Digital Design and Design Environments: (08 hours)

Design, Hierarchy, Views, Connectivity, Spatial Dimensionality, Introduction of Design Environments, System Level, Algorithm Level, Component Level, Layout Level

UNIT II

Representation: **(08 hours)**

Introduction, General Issues of Representation, Hierarchy Representation, View Representation, Connectivity Representation, Geometry Representation.

UNIT III

Synthesis Tools: **(08 hours)**

Introduction, Cell Contents Generation and Manipulation, Generators of Layout outside the Cells, Cells and Their Environment, Silicon Compilers, Post layout Generators,

UNIT IV

Static Analysis Tools, Dynamic Analysis Tools: **(08 hours)**

Node Extraction, Geometrical Rule Checker, Electrical Rule Checker, Verification, Circuit–Level Simulators, Logic-Level Simulators, Functional and Behavioral Simulation Issues, Event Driven and Hardware Simulation

UNIT V

Output of Design Aids and Programmability: **(08 hours)**

Introduction, Circuit Boards, Integrated Circuits, Implementation Issues, Imperative Programming, Declarative Programming, Hierarchy.

UNIT VI

Graphics and Human Engineering: **(08 hours)**

Introduction, Display Graphics, Hardcopy Graphics, Input Devices, Task and User Modeling, Information Display, Command Language Feedback.

Book:

1. M.J.S. Smith. Application-Specific Integrated Circuits. Addison Wesley.

Bharati Vidyapeeth
(Deemed to be University)
College of Engineering, Pune

Self-Study Paper II: HUMAN VALUES & PROFESSIONAL ETHICS

TEACHING SCHEME

Lectures: 04 Hrs/Week

EXAMINATION SCHEME

Duration: 03 Hrs

Theory: 60 Marks

Internal Assessment: 40 Marks

Total Credits: 04

Course prerequisites:

- Listening skills for academic and professional purposes.
- Ability to speak effectively in English in real-life situations.

Course objective:

1. To create awareness on engineering ethics and human values
2. To understand social responsibility of an engineer
3. To appreciate ethical dilemma while discharging duties in professional life

---

Course Outcomes: On successful completion of this course, students will be able to

1. Familiar with the ethical issue and professional issue in the engineering profession.
2. Familiar with social impact of decision and the action of participants in the engineering profession

---

Contents

UNIT I (08 Hours)

Human Values

Morals, Values and Ethics - Integrity, - Work Ethics - Service Learning - Civic Virtue -Respect for others - Living Peacefully - Caring - sharing - Honesty - Courage - Valuing Time- Cooperation - Commitment - Empathy – Self-Confidence - Character - spirituality

UNIT II (08 Hours)

Engineering Ethics

Senses of engineering ethics - Variety of Moral Issues - Types of inquiry - Moral Dilemmas Moral Autonomy - Kohlberg's Theory - Gilligan's Theory - Consensus and Controversy - Models of Professional Roles - Theories about Right Action - Self-Interest - Customs and Religion .

UNIT III (08 Hours)

Safety, Responsibilities and Rights

Safety and Risk - Assessment of safety and Risk - Risk Benefit Analysis and Reducing Risk - The Three Mile Island. And Chernobyl Case Studies. Collegiality and Loyalty - Respect for Authority - Collective Bargaining - Confidentiality - Conflicts of Interest - Occupational Crime - Whistle Blowing - Professional Rights – Employee Rights - Intellectual Property Rights (IPR) – Discrimination

UNIT IV (08 Hours)

Global Issues

Multinational Corporations - Environmental Ethics - Computer Ethics - Weapons Development - Engineers as Managers - Consulting Engineers - Engineers as Expert Witnesses and Advisors - Sample Code of Ethics of ASME, ASCE, IEEE, Institution of Engineers (India), etc.

UNIT V (08 Hours)

Engineer's responsibility for safety

Collegiality and loyalty-respect of authority-collective bargaining-confidentiality-conflicts of interest-occupational crime- professional rights-employee rights-Intellectual property rights (IPR).

UNIT VI (08 Hours)

Engineering as social Experimentation

Engineering as social experimentation-engineers as responsible experimenters-codes of ethics-a balanced outlook on law- the challenger case study

Text Books/ References:

- Bayles, M.D.: Professional Ethics, California: Wadsworth Publishing Company, 1981.
- Koehn, D.: The Ground of Professional Ethics, Routledge, 1995.
- R.S. Naagarazan, A Text Book of Professional Ethics & Human Values, New Age
- International, 2006 . Mike Martin and Ronald Schinzinger, Ethics in Engineering",McGraw-Hill,New YORK1996
- Camenisch, P.F.: Grounding Professional Ethics in a Pluralistic Society, N.Y.: Haven Publications, 1983.
- Wuest, D.E. : Professional Ethics and Social Responsibility, Rowman & Littlefield, 1994.

Bharati Vidyapeeth
(Deemed to be University)
College of Engineering, Pune

Self-Study Paper II: VLSI Signal Processing

TEACHING SCHEME

Lectures: 04 Hrs/Week

EXAMINATION SCHEME

Duration: 03 Hrs

Theory: 60 Marks

Internal Assessment: 40 Marks

Total Credits: 04

Course prerequisites:

- Basic Electronics.
- Electronic Devices
- Digital Signal Processing

Course objective:

1. Different representation techniques that DSP algorithms employ.
2. Apply the architectural transformation techniques.
3. Signify and calculate the effects of scaling and round-off noise for a digital filter with limited word length

---

Course Outcomes: On successful completion of this course, students will be able to

1. Compare various representation methods of DSP algorithms.
2. Find the iteration bound of a given single and/or multi-rate DFG.
3. Transform the given DFG using retiming with constraints.
4. Apply unfolding and folding transformations to the given DFG
5. Apply algorithmic and numerical strength reduction methods.
6. Calculate the scaling and round-off noise of the given digital filter with a limited word length.

Contents

UNIT I (08 Hours)

Introduction to Digital Signal Processing

Typical DSP Algorithms, DSP Application Demands and Scaled CMOS Technologies, Representations of DSP Algorithms, Data-Flow Graph Representations

UNIT II (08 Hours)

Iteration Bounds

Loop Bound and Iteration Bound, Algorithms for ComputingIteration Bound: Longest Path Matrix and Multiple Cycle Mean algorithms - Iteration Bound of Multi-rate Data Flow Graphs

UNIT III (08 Hours)

Pipelining, Parallel processing and Retiming

Pipelining and Parallel Processing, Introduction to Retiming, Definitions and Properties, Solving Systems of Inequalities, The Bellman-Ford Algorithm, The Floyd Warshall Algorithm, Retiming Techniques.

UNIT IV (08 Hours)

Unfolding and folding

An Algorithm for Unfolding, Properties of Unfolding, Critical Path, Unfolding, and Retiming, Applications of Unfolding. Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures.

UNIT V (08 Hours)

Algorithmic & Numerical Strength Reduction

Introduction to Algorithmic Strength Reduction, Cook-Toom Algorithm, Iterated Convolution, Cyclic Convolution, Discrete Cosine Transform. Introduction to Numerical Strength Reduction, Canonic Signed Digit Arithmetic, Sub-expression Elimination, Multiple Constant Multiplication, Sub-expression,Sharing in Digital Filters

UNIT VI (08 Hours)

Scaling and Rounding Noise

Scaling and Rounding Noise, State Variable Description ofDigital Filters, Scaling and Rounding Noise Computation,Rounding Noise in Pipelined IIR Filters.

Text Books/ References:

1. Parhi, Keshab K. VLSI digital signal processing systems: design and implementation.
2. Proakis, John G. Digital signal processing: principles, algorithms, and applications, 4/E.
3. Kalya, Shubhakar, Muralidhar Kulkarni, and K. S. Shivaprakasha, eds. Advances inCommunication, Signal Processing, VLSI, and Embedded Systems: Select Proceedings of
4. Mitra, Sanjit Kumar. Digital signal processing: a computer-based approach. Vol. 1221.


BHARATI VIDYAPEETH
UNIVERSITY
PUNE

BHARATI VIDYAPEETH
(DEEMED TO BE UNIVERSITY), PUNE

Faculty of Engineering And Technology
M.Tech. - Electronics
Old Syllabus

Structure of M.Tech Electronics Engineering (VLSI)

Based on Credit Pattern

STRUCTURE & EXAMINATION PATTERN

Semester I											**Total Duration: 20 hrs/week** **Total Marks :500** **Total Credits: 18**
Subject	**Teaching Scheme (Hrs)** **Hrs./Week**		**Examination Scheme** **(Marks)**						**Examination Scheme** **(Credits)**		**Total Credits**
	L	**P**	**Theory**	**Unit Test**	**Attendance**	**Tutorial/assignments**	**TW**	**Pract/ Oral**	**TH**	**TW/PR /OR**	
Digital VLSI design	04	02	60	20	10	10	25	25	04	01	05
Embedded System & processors	04	02	60	20	10	10	25	25	04	01	05
Advanced Digital communication system	04	--	60	20	10	10	--	--	04	--	04
Linear algebra & random processes	04	--	60	20	10	10	--	--	04	--	04
Total	**16**	**06**	**240**	**80**	**40**	**40**	**50**	**50**	**16**	**02**	**18**

Semester II									**Total Duration: 20 hrs/week** **Total Marks :500** **Total Credits: 18**		
Subjects	**Teaching Scheme (Hrs)** **Hrs./Week**		**Examination Scheme** **(Marks)**						**Examination Scheme** **(Credits)**		**Total Credits**
	L	**P**	**Theory**	**Unit Test**	**Attendance**	**Tutorial/ assignments**	**TW**	**Pract/ Oral**	**TH**	**TW/PR/ OR**	
Analog VLSI Design	04	02	60	20	10	10	25	25	04	01	05
Advanced digital signal processing	04	02	60	20	10	10	25	25	04	01	05
Wireless Networks	04	--	60	20	10	10	--	--	04	-	04
Image & video processing	04	--	60	20	10	10	--	--	04	--	04
Total	**16**	**04**	**240**	**80**	**40**	**40**	**50**	**50**	**16**	**02**	**18**

M.Tech.(Electronics) Sem-I

Bharati Vidyapeeth Deemed University,
College of Engineering, Pune

ADVANCED DIGITAL COMMUNICATION SYSTEM

TEACHING SCHEME

Lectures: 04 Hrs/Week

EXAMINATION SCHEME

Duration: 03 Hrs

Theory : 60 Marks

Internal Assessment: 40 Marks

Total Credits: 04

Course prerequisites:
Knowledge of random processes and linear system theory (Transforms, convolution, sampling)

Course objective:

To provide students with the knowledge & understanding of modern communication systems.

Course Outcomes: Upon Completion of the course, the students will be able to

1. To identify and describe different techniques in modern communication systems.
2. To understand the basic theory of modulation & demodulation techniques.
3. To possess knowledge of different codes.
4. To apply fundamentals of communication systems to solve the Engineering Problems.

Contents:

UNIT I (08 Hours)

Basic digital pass band modulation

Introduction, Binary amplitude shift keying(BASK), Binary Phase shift keying(BPSK), Binary frequency shift keying(BFSK),Performance comparison of BASK, BFSK,BPSK, Digital modulation techniques for spectral efficiency, Quadrature Phase shift keying(QPSK),

Offset Quadrature Phase shift keying(OQPSK), Minimum shift keying(MSK),Comparison of M-ary signaling techniques.

UNIT II (08 Hours)

Demodulation:
The matched filter, The correlator, envelop detector, output signal to noise ratio, Binary demodulation, coherent PSK,DPSK,FSK, non-coherent FSK,DPSK ,MSK .

UNIT III (08 Hours)

Channel coding
Reed soloman codes, Interleaving & concatenated codes, coding and Interleaving applied to the compact disc digital audio system, Linear block codes, Cyclic Redundancy check (CRC), Turbo codes, Automatic repeat request (ARQ).

UNIT IV (08 Hours)

Fading Channels
Multipath propagation, Flat & frequency selective fading, Fast and slow fading Random channel models, Signal design for radio channels, Diversity, Modulation, Coding.

UNIT-V (08 Hours)

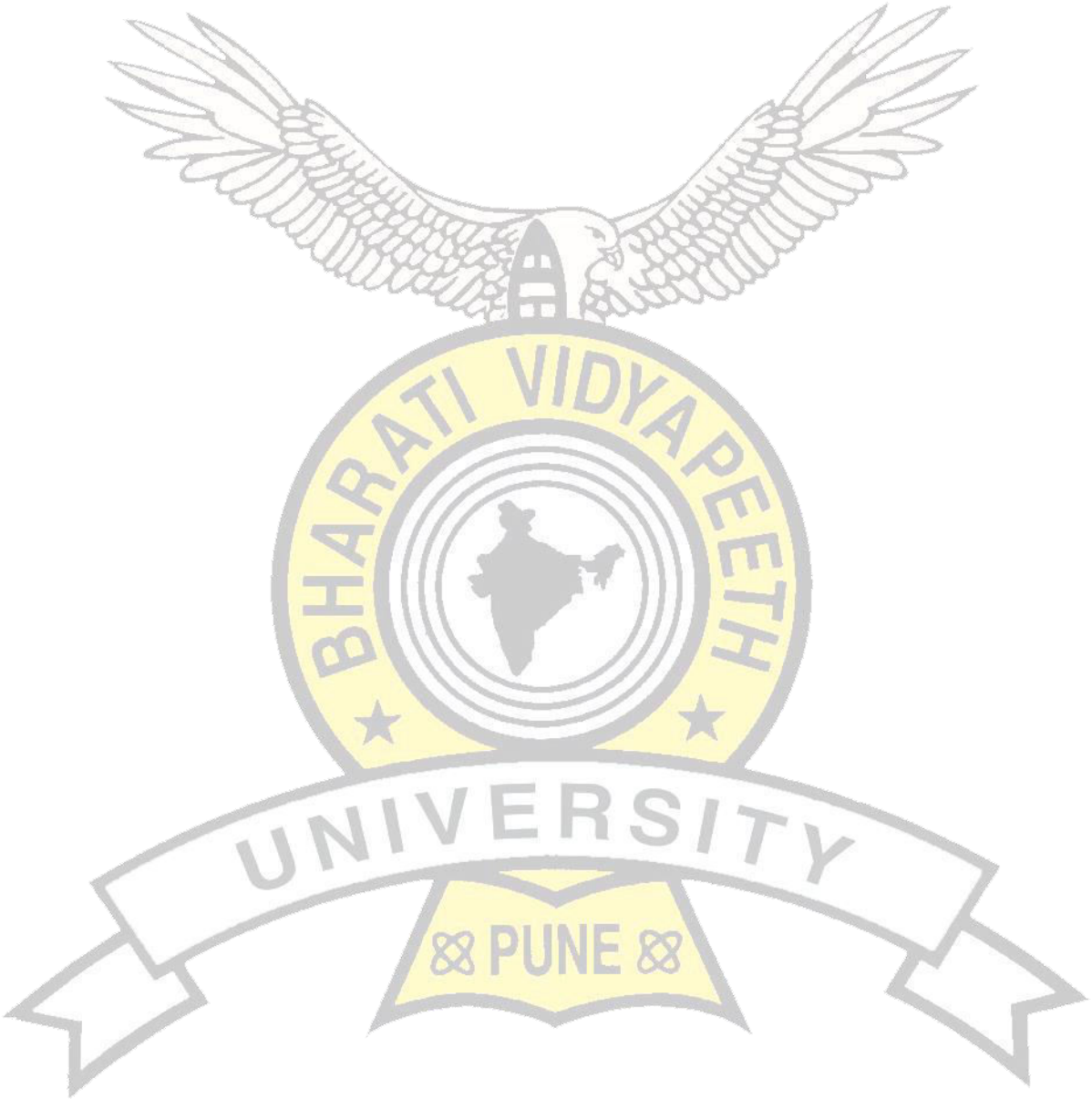
Advanced Modulation techniques
Trellis –coded modulation, Direct sequence modulation, IS-95 forward link, Code division multiple Access (CDMA), IS-95 reverse link, Frequency hop Spread Spectrum (FH-SS) ,CDMA, Pseudorandom sequences: generation & properties, Rake receiver

UNIT VI (08 Hours)

OFDM
Introduction to OFDM, Low mobility, High mobility, Time diversity, Frequency diversity, Receiver antenna diversity (SIMO), Transmit antenna diversity (MISO), Transmit receive antenna diversity.

Text Books/ References:

1. Digital communications- Simon Haykin, John Wiley and sons, 1998
2. Digital Communications- Bernard Sklar, Second edition, Pearson Education, 2001.
3. Nguyen Ha, Shwedyk Ed, " A First Course in Digital Communications, Cambridge University Press.
4. Digital communication, 4th ed. - J. G. Proakis, MGH International edition.
5. Principle of Communication Systems – Taub, Schilling, TMH
6. Communication Systems, 4th ed. – A. Bruce Carlson, Paul B. Crilly, Janet C. Rutledge, MGH International edition.
7. Advanced Digital Communication Sytems-NIIT,PHI learning.


BHARATI VIDYAPEETH
UNIVERSITY
PUNE

DIGITAL VLSI DESIGN

TEACHING SCHEME

Lectures: 04 Hrs/Week

Practicals: 02 Hrs/Week

EXAMINATION SCHEME

Duration: 03 Hrs

Theory : 60 Marks

InternalAssessment:40 Marks

TW&OR:50 Marks

Total Credits: 05

Course Prerequisite:

Knowledge of Digital Electronics

Course Objective:

To understand theory and to learn design of digital system. The course will involve design and simulation of digital circuits using VHDL

Course Outcomes: On successful completion of this course, students will be able to

- Ability to apply various modeling styles for digital circuits.
- Ability to design sequential and combinational circuits using VHDL.
- Ability to conceptualize FSM.
- Ability to simulate digital circuits.
- Ability to apply concepts of PLD designs.

Contents:

UNIT I (08 Hours)

VHDL Basics

Objectives of VHDL, Entity-Architecture Concepts, Introduction to various modeling styles of VHDL (Behavioral, Dataflow, Structural and Mixed), VHDL Basic Elements (Data types, Data objects and Operator), Configuration, Package declaration.

UNIT II (08 Hours)
VHDL Modeling-1

Dataflow Modeling: Example based on dataflow modeling, When-Else and With Select Statement, Concept of Delta delay and multiple drivers, Generate and Block Statements
Structural modeling: Concept of Component

UNIT III (08 Hours)

VHDL Modeling-2

Behavioral and mixed modeling for digital design, If-else, Loop, Case, Assert and Report statements, State Machine Design, Moore and Mealy FSM Design using VHDL

UNIT IV (08 Hours)

EDA tools

Digital Design Flow, RTL Synthesis, Synthesis Flow, Functional and Timing simulation, Physical Verification, Floor planning, Place and route, IP Design

UNIT V (08 Hours)

Programmable Logic Devices

Overview of PLDs, SPLD, CPLD, FPGA, Case study of Xilinx family XC 4000 and XC9500, Modes of configuration.

UNIT VI (08 Hours)

Designing with PLDs

Designing with ROM, PLA, PAL, GAL, CPLD and FPGA, Implementing functions in PLDs.

Text Books/ References:

1. VHDL: Programming by Example-Douglas Perry, McGraw Hill, Fourth Edition, 2002.
2. Fundamentals of Logic Design-Charles Roth, Larry Kinney, Cengage Learning, Seventh edition, 2014.
3. A VHDL Primer-J. Bhaskar, PHI Learning, Third Edition, 1998.
4. CMOS VLSI Design: A Circuits and system perspectives- Neil H.E. Weste, Davir Harris, Pearson Education 3rd Edition, 2004.

5. Circuit Design and Simulation with VHDL- V. Pedroni, MIT Press, Second Edition, 2010

Text Books:

1. R.P. Jain , "Modern digital electronics" , 3rdedition , 12th reprint TMH Publication, 2007.
2. Anand Kumar 'Fundamentals of Digital Circuits'--. PHI

Reference Books :

1. J.F.Wakerly "Digital Design: Principles and Practices", 3rd edition, 4th reprint, Pearson Education, 2004.
2. A.P. Malvino, D.P. Leach 'Digital Principles & Applications'' –Vith Edition-Tata Mc Graw Hill, Publication.
3. Morris Mano 'Digital Design'-- (Third Edition),.PHI

Bharati Vidyapeeth Deemed University,
College of Engineering, Pune

EMBEDDED SYSTEMS AND PROCESSORS

TEACHING SCHEME

Lectures: 04 Hrs/Week

EXAMINATION SCHEME

Duration: 03 Hrs

Theory : 60 Marks

Internal Assessment: 40 Marks

TW&OR:50 Marks

Total Credits: 04

Course Prerequisites:

Knowledge of microcontrollers like 8051, PIC and ARM

Course objective:

- To understand need and application of ARM Microprocessors in embedded system.
- To understand architecture and features of typical PSoC.
- To learn the importance of interprocess communication.
- To learn Real time operating system and its application.

Course Outcomes: After successfully completing the course students will be able to

- Describe the PSoC architectures and its feature.
- Interface the advanced peripherals to ARM based microcontroller.
- Design embedded system with available resources.

Contents:

UNIT I (08hours)

ARM7 & ARM 9 Based Microcontroller

Review of ARM7, ARM9, &ARM11 processors .
Interfacing of ARM7 & ARM 9 processors with real world: LED, LCD, KEYPAD,SDI card,UART.

UNIT II (08hours)

Interprocess Communication

Multiple processes in an application, problem of shared data, interprocess communication, RTOS task scheduling, interrupt latency and response time, interrupt service mechanism Context and context switching.

UNIT III (08hours)

Real Time systems

Kernel, Scheduler, Non-Preemptive Kernel , Preemptive Kernel, Reentrancy, Round robin scheduling, Task Priorities, Static & Dynamic Priority, Priority Inversion, Assigning task priorities, Mutual Exclusion, Deadlock, Clock Tick, Memory requirements, Advantages & disadvantages of real time kernels

UNIT IV (08hours)

Introduction to PSoC

PSoC technology, programmable routing and interconnect, configurable analog and digital blocks, cpu sub system, families of PSoC .

PSoC 3/5, architecture – block diagram, system wide resources, I/O interfaces, CPU sub system,

memory organization, digital sub systems, analog sub systems

UNIT V (08hours)

PSoC components:

Universal digital blocks (UDB), UDB arrays and counter and PWM, digital filter gain amplifiers, switched capacitor / continuous time, analog routing, flash temperature sensors,DTMF dialers, sleep timers, UART, I2 C, SPI,USB,CAN buses.

UNIT VI (08hours)

µCOS II

Features of. Kernel structure. µCOS II RTOS services:Task management, Time management, Intertask Communication and Synchronization.

Text Books:

1. Andrew Sloss, Dominic Symes. Chris Wright,'ARM System Developer s Guide-Designing and Optimizing System Software', ELSEVIER
2. Joseph Yiu,'The Definitive Guide to the ARM Cortex –M',ELSEVIER
3. Rajkamal ,'Embedded System –Architecture, Progrmming and design,'TMH Publication,edition2003
4. PSoC 3, PSoC 5 Architecture technical reference manual, Cypress website
5. Robert Asbhby, My First Five PSoC 3 design (e-book), , Cypress website

Reference Books:

1. LPC 214x User manual (UM10139);-www.nxp.com
2. LPC17xx User manual (UM10360);-www.nxp.com
3. ARM architecture reference manual:-www.arm.com
4. Trevor Martin,' An Engineer's Introduction to the LPC2100 Series', Hitex (UK) Ltd.
5. Designer Guide to the Cypress PSoC, Robort Ashby, Elsevier Publications
6. Introduction to Mixed Signal Embedded Design, Alex Doboli, Springer
7. The Beginners Guide to Using PSoC Express: Mixed-Signal Microcontroller Development without Code, Oliver H. Bailey, Timelines Industries Incorporated, 2007
8. PSoC Mikrocontroller by Fredi Kruger Franzis, 2006

• **Web References:**

1. www.cypress.com/go/psoc
2. www.cypress.com/go/trainning
3. www.cypress.com/go/support
4. www.psocdeveloper.com

Bharati Vidyapeeth Deemed University,
College of Engineering, Pune

LINEAR ALGEBRA AND RANDOM PROCESS

TEACHING SCHEME

Lectures: 04 Hrs/Week

EXAMINATION SCHEME

Duration: 03Hrs

Theory: 60 Marks

Internal Assessment: 40 Marks

Total Credits: 04

Course prerequisites:

Knowledge of Grouo theory, ring theory,Field theory

Course objective:

- To develop the ability to use the concepts of linear algebra and special functions for solving problems to related networks
- To formulate and construct a mathematical model for linear programming problem in real life situations

---

Course Outcomes: On successful completion of this course, students will be able to

- To achieve and understanding of the basic concepts of algebraic equations and methods of solving them
- To familiarize the students with special functions and solve problems associated with engineering applications

Contents:

UNIT I (08 Hours)

LINEAR Algebra:

Vector spaces-norms-inner products-Eigen values using QR transformations-QR factorization-generalized eigenvectors-canonical forms-singular value decomposition and applications-pseudo inverse-least square approximation-Toeplitz matrices and some applications

UNIT II (08 Hours)

LINEAR PROGRAMMING:

Formulation-graphical solution-simplex method-Two phase method-Transportation and assignment models , Efficient computational algorithms , Duality, Parametric Linear programming, integer Linear Programming.

UNIT III (08 Hours)

ORIDINARY DIFFERENTIAL EQUATIONS:

Runge-kutta methods for system of IVP's , numerical stability, Adamas-Bashforth multistep methop, solution of stiff ODE's shooting method, BVP: Finite difference method, orthogonal collocation method, orthogonal collocation with finite element method, Galerkin finite element method

UNIT IV (08 Hours)

TWO DIMENSIONAL RANDOM VARIABLES:

Joint distributions- marginal and conditional distributions- functions of two dimensional random variables- regression curve- correlation.

UNIT V (08 Hours)

QUEUEING MODELS:

Poisson's process- Mark ovian queues- single and multi server models- little's formula – machine interference model- steady state analysis- self service queue. Pure Birth and Death Models (Relationship between the Exponential And Poission Distribution.)

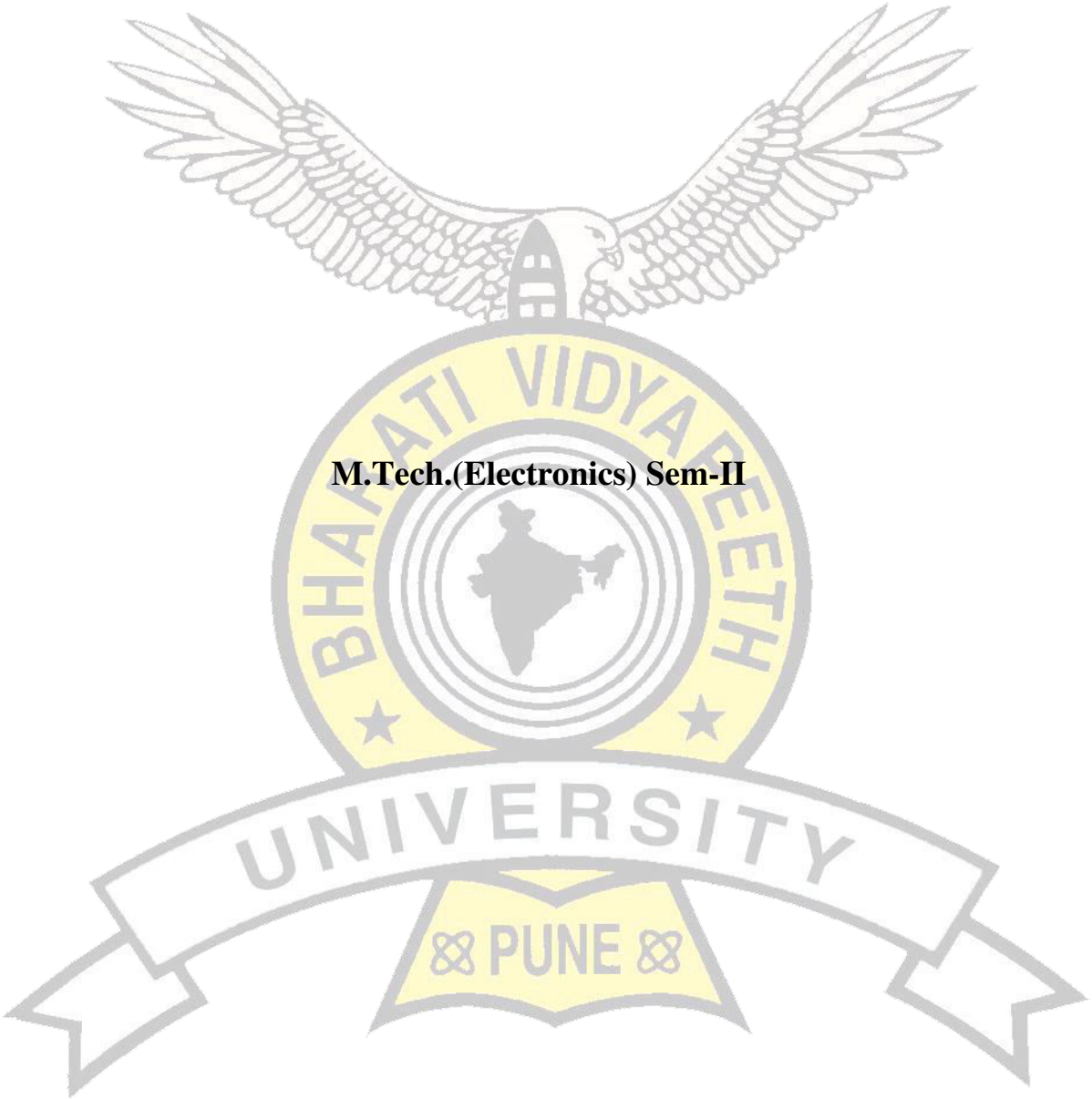
UNIT VI (08 Hours)

RANDOM PROCESS:

Averages of a random process, stationary random process, ergodic random process, random process-mean and covariance unction, linear filtering of random process, power spectral density, spectral analysis of random process, Gaussian Poisson random process.

Text Books/ References:

1. Richard Bronson, Gabriel B. Costa, " Linear Algebra", Academic press, Second edition, 2007
2. Richard Johnson, Miller and Freund, "Probability and Statics for Engineers", Seventh edition, Prentice-Hall of India, private limited, New Delhi (2007)
3. Taha H. A. " Operations research, and Introduction", Pearson Eductaion Asia, New Delhi, Ninth edition, 2012
4. Donald Gross and Carl M. Harris," Fundamentals of Queueing theory" Second Edition, John Wiley and sons, Newyork (1985)
5. Moon, T. K. ,Sterling, W. C. , Mathematical Methos and algorithms for signal processing, Pearson Education, 2000
6. Oliver C. Ibe, "Fundamentals of applied probability and random process", Elsevier, First Indian reprint, 2007
7. Linear Algebra , "Pist and Sahai".



M.Tech.(Electronics) Sem-II

Bharati Vidyapeeth Deemed University,
College of Engineering, Pune

ADVANCED DIGITAL SIGNAL PROCESSING

TEACHING SCHEME
Lectures: 04 Hrs/Week
Practicals:2Hrs/Week

EXAMINATION SCHEME
Duration: 03 Hrs
Theory: 60 Marks
Internal Assessment: 40 Marks
TW&OR:50 Marks

Total Credits: 05

Course objective:

- This course covers the fundamental aspects of digital signal processing.
- To introduce the various techniques that is fundamental to a variety of application areas.

Course Outcomes: On successful completion of this course, students will be able to

1. To apply fundamental mathematical tools, in the analysis and design of signal processing systems.
2. To identify estimation problems and design, implement algorithms for solving them.
3. To understand the basic theory of wavelet transform and the concepts of using Simple wavelets for simple applications.

Contents:

UNIT I (08 Hours)

Linear Prediction:

Forward and Backward Linear prediction, optimum reflection coefficient for lattice backward and forward prediction, solution of normal equations (Levinson-Durbin algorithm and Schur algorithm), properties of linear prediction filters.

UNIT II (08 Hours)

Adaptive Filters:

Applications of adaptive filters: System identification, adaptive channel equalization echo cancellation in data transmission over telephone channels, linear predictive coding of speech signals, adaptive direct form filters-LMS algorithm, RLS algorithm.

UNIT III (08 Hours)

Power Spectrum Estimation:

Estimation of power spectrum and correlation, Non-parametric and parametric methods, Minimum Variation Estimation methods, Eigen Analysis algorithm, Power Spectrum analysis using DFT.

UNIT IV (08 Hours)

Programmable Digital Signal Processors:

Multiplier accumulator unit (MAC), modified bus structures, Multiple Access memory, VLIW architecture, pipelining, special addressing modes in P-DSP's.

UNIT V (08 Hours)

An Overview of TMS320C6X DSPs:

Introduction, features of TMS320C6X processors, Internal Architecture, CPU & data paths, Addressing modes, memory architecture, pipeline, peripherals, program development.

UNIT VI (08 Hours)

Wavelet Transforms:

Fourier Transform and its limitations, Short Time Fourier Transform, Continuous Wavelet Transform,Discretization of the Continuous wavelet Transform,Multiresolution Approximations; wavelet and Scaling Function Coefficients,Orthonormality of Compactly Supported Wavelets,Bi-orthogonal Decomposition,Harr wavelets, The Daubechies Wavelets Construction, Fast Wavelet Transform and Image Compression,Denoising using wavelets, Perfect Reconstruction Filter bank design using Wavelets.

Text Books/References:

1. Digital Signal Processing Using MATLAB by V.K.Ingle and J.G.Prokais (Books/Colle,2000)
2. Digital Signal Processing:Principles,Algorithms and Applications by J.G.Prokais and D.G.Manolakis

Bharati Vidyapeeth Deemed University,
College of Engineering, Pune

ANALOG VLSI DESIGN

TEACHING SCHEME

Lectures: 04 Hrs/Week

Practicals: 02 Hrs/Week

EXAMINATION SCHEME

Duration: 03 Hrs

Theory : 60 Marks

Internal Assessment: 40 Marks

TW&OR:50 Marks

Total Credits: 05

Course prerequisites:

Basic Electronics and Physics

Course objective:

To understand theory and to learn design of analog systems at transistor level. The course will involve design, layout and simulation of analog VLSI circuits using various CAD tools.

Course Outcomes: On successful completion of this course, students will be able to

- Ability to apply modeling for MOS circuits.
- Ability to design Analog CMOS sub-circuits.
- Ability to conceptualize CMOS amplifiers.
- Ability to characterize CMOS Op-amps.
- Ability to apply concepts of Switched Capacitor Circuits.

Contents:

UNIT I (08 Hours)

MOS Devices and Modeling

The MOS Transistor, CMOS Device Modeling -Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Sub-threshold MOS Model.

UNIT II (08 Hours)

Analog CMOS Sub-Circuits

MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors, Current and Voltage References, Band gap Reference.

UNIT III (08 Hours)

CMOS Amplifiers

Inverters, Differential Amplifiers, Cascode Amplifiers

UNIT IV (08 Hours)

CMOS Operational Amplifiers

Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power-Supply Rejection Ratio of Two -Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

UNIT V (08 Hours)

High Performance CMOS OP AMP

High Speed/Frequency OP AMP, Micro Power OP AMP, Low Noise OP AMP, Low Voltage OP AMP.

UNIT VI (08 Hours)

Switched Capacitor Circuits

Switched Capacitor Circuits Switched Capacitor Amplifiers, Switched Capacitor Integrators.

Text Books/ References:

1. CMOS Analog Circuit Design -Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Analysis and Design of Analog Integrated Circuits -Paul R. Gray, Paul J. Hurst, S. Lewis and
R. G. Meyer, Wiley India, Fifth Edition, 2010.
3. Analog Integrated Circuit Design-David A. Johns,Ken Martin, Wiley Student Edn, 2013
4. Design of Analog CMOS Integrated Circuits-Behzad Razavi, TMH Edition, 2002.
5. CMOS: Circuit Design, Layout and Simulation-Baker, Li and Boyce, PHI, 2010.

Bharati Vidyapeeth Deemed University,
College of Engineering, Pune

DIGITAL IMAGE AND VIDEO PROCESSING

TEACHING SCHEME
Lectures: 04 Hrs/Week

EXAMINATION SCHEME
Duration: 03 Hrs
Theory: 60 Marks
Internal Assessment: 40 Marks
Total Credits: 04

Course objective:

- This course provides an introduction to basic concepts, algorithms of digital image and video processing.
- To provide different analytical tools and methods applied in Digital Image processing

---

Course Outcomes: On successful completion of this course, students will be able to

- To apply principles and techniques of digital image processing in applications related to digital imaging system.
- To use and implement basic algorithms for image & video compression

Contents:

UNIT I (08 Hours)

Fundamentals of Image processing

Introduction to Digital Image Processing : Digital image fundamentals:, Applications of Image Processing, Simple image formation model, Image sampling and quantization - Basic relationships between pixels, connectivity, adjacency. Distance between the pixels . Elements of human visual perception, MTF, Image statistics.

.

UNIT II (08 Hours)

Image Enhancement

Image Enhancement: Spatial domain methods: point processing - intensity transformations, histogram processing, image subtraction, image averaging; Image zooming, Spatial filtering - smoothing filter, sharpening filter. 2D-DFT, FFT, Frequency domain filtering: low pass filtering, high pass filtering, and Homomorphic filtering.

UNIT III (08 Hours)

Image Compression

Image Compression: Fundamentals, Lossless Compression schemes like Huffman, Arithmetic ,LZW and lossless Prediction. 2D-DCT, KL, Hadamard Image compression using DCT, zig-zag scanning, still image compression standard - baseline JPEG. Vector Quantization

UNIT IV (08 Hours)

Image Segmentation

Image Segmentation: Fundamentals, point, line and edge and combined detection, Thresholding Edge linking Hough transform, Region oriented segmentation - basic formulation, region growing by pixel aggregation, region splitting and merging, Segmentation using watersheds

UNIT V (08 Hours)

Image Restoration

Morphological Operations: Erosion and Dilation, Opening and Closing, Hit and Miss transform, Boundary extraction, region filling, Extraction of connected components.
Image Restoration: Image degradation/restoration model, Noise models, Linear Position invariant degradation, Estimation of degradation function, inverse filtering, Wiener filter.

UNIT VI (08 Hours)

An overview of Video processing

Analog Video, Digital Video, Motion estimation and detection, video enhancement, Video compression fundamentals.

Text Books/References:

1. Gonzalez and Woods, "Digital Image Processing", 3rd Edition, Pearson Education.
2. Pratt William K. "Digital Image Processing", John Wiley & sons .
3. S. Jayaraman, S. Esakkiraian “Digital Image Processing”, Tata McGraw-Hill Education .
4. Al.Bovik,” Handbook of Image and Video Processing “ Academic Press.
5. B,Chanda and D.Datta Mujumdar “ Digital Image Processing and Analysis”, Prentice Hall of India.
6. Madhuri Joshi,” Digital Image Processing” Prentice Hall of India.
7. Joshi, Madhuri A., Mehul S. Raval, Yogesh H. Dandawate, Kalyani R. Joshi, and Shilpa P. Metkar. *Image and Video Compression: Fundamentals, Techniques, and Applications*. CRC Press, 2014.

Bharati Vidyapeeth Deemed University,
College of Engineering, Pune

WIRELESS NETWORKS

TEACHING SCHEME

Lectures: 04 Hrs/Week

Practical: --Hrs/Week

EXAMINATION SCHEME

Duration: 03 Hrs

Theory: 60 Marks

Internal Assessment: 40 Marks

Total Credits: 04

Course objective:

- To introduce the concepts and techniques associated with Wireless Cellular Communication systems.
- To familiarize with state of art standards used in wireless cellular systems.

To understand the concept of new technologies in wireless systems

---

Course Outcomes: On successful completion of this course, students will be able to

1. Explain the Classification of mobile communication systems
2. Analyze the radio channel characteristics and the cellular principle
3. Ability to analyze improved data services in cellular communication

Contents:

UNIT I (08 Hours)

Introduction

Systems and Design Fundamentals, Propagation Models Description of cellular system, Frequency Reuse, Co channel and Adjacent channel interference, Propagation Models for Wireless Networks, Multipath Effects in Mobile Communication, Models for Multipath Reception.

UNIT II (08 Hours)

Cellular Communications

Introduction to Cellular Communications, Frequency reuse, Multiple Access Technologies, Cellular Processes-Call Setup, Handover etc, Teletraffic Theory, Capacity Building, Blocking Probability

UNIT III (08 Hours)

CDMA

Introduction to CDMA, Walsh codes, Variable tree OVSF, PN Sequences, Multipath diversity, RAKE Receiver, CDMA Receiver Synchronization

UNIT IV (08 Hours)

GSM

Architecture and Protocols - Air Interface, GSM Multiple Access Scheme, GSM Channel Organization, Traffic Channel multiframe, Control (Signaling) Channel Multiframe, Frames, Multi-frames, Super-frames and Hyper-frames, GSM Call Set up Procedure, GSM Protocols and Signaling, Location Update Procedure, Routing of a call to a Mobile Subscriber.

UNIT V (08 Hours)

MIMO

Introduction to MIMO, MIMO Channel Capacity, SVD and Eigen modes of the MIMO Channel, MIMO Spatial Multiplexing – BLAST, MIMO Diversity – Alamouti, MIMO Diversity-OSTBC, MIMO Beam Forming-MRT, MIMO - OFDM

UNIT VI (08 Hours)

3G and 4G Wireless Standards/UWB

GPRS, WCDMA, LTE, WiMAX, UWB Definition and Features, UWB Wireless Channels, Bit-Error Rate Performance of UWB

Text Books/ References:

1. Wireless Communications, Principles, Practice – Theodore, S. Rappaport, 2nd Ed.2002, PHI.
2. Wireless Communications-Andrea Goldsmith, 2005 Cambridge University Press.

3. Mobile Cellular Communication – Gottapu Sasibhushana Rao, Pearson Education, 2012.
4. Principles of Wireless Networks – Kaveh Pah Laven and P. Krishna Murthy, 2002
5. Wireless Digital Communications – Kamilo Feher, 1999, PHI.
6. Wireless Communication and Networking – William Stallings, 2003, PHI.
7. Wireless Communication – Upen Dalal, Oxford Univ. Press
8. Wireless Communications and Networking – Vijay K. Gary, Elsevier.

Bharati Vidyapeeth Deemed University,
College of Engineering, Pune
Structure of M.Tech (Electronics -VLSI)
Based on Credit Pattern

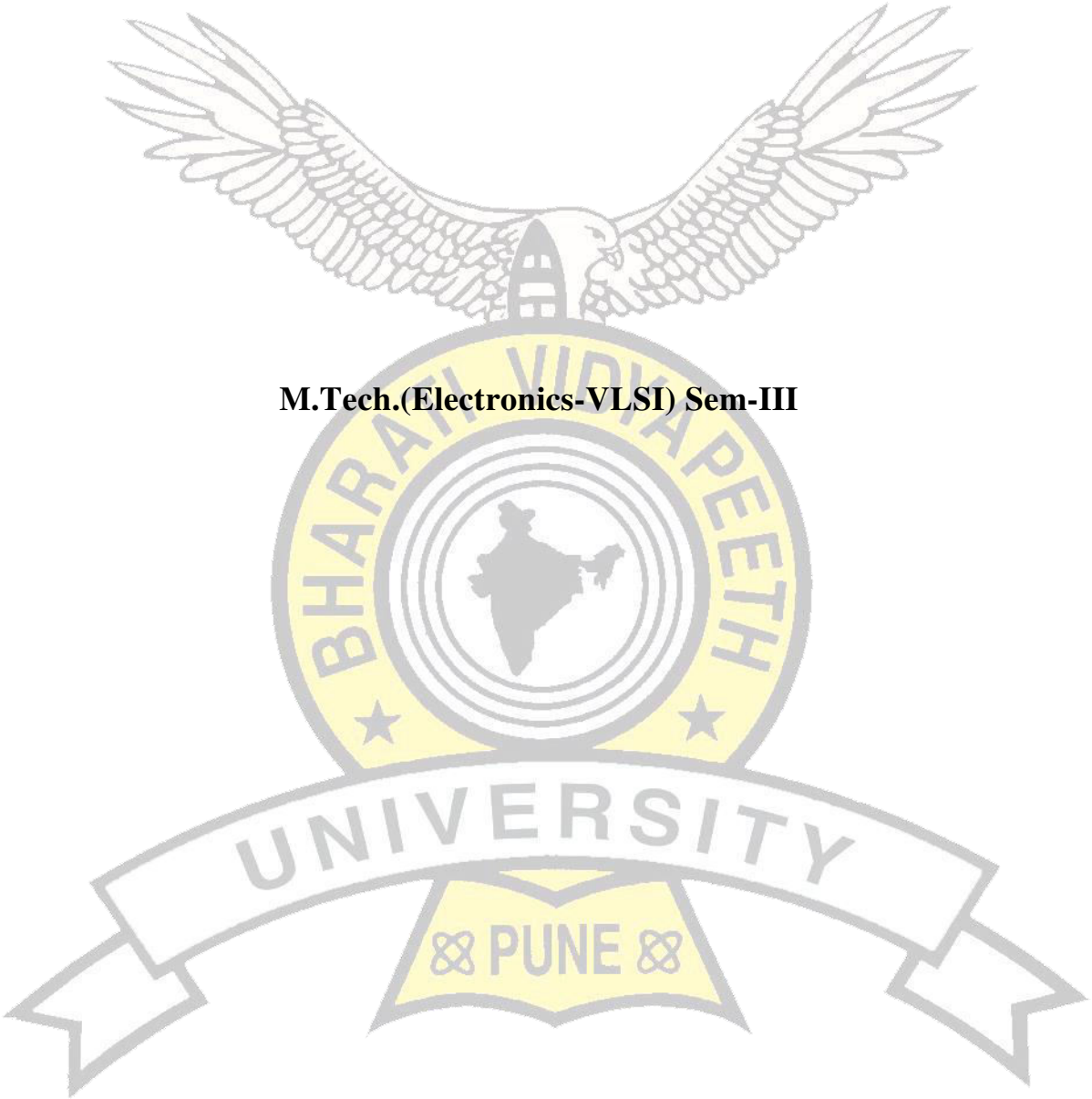
Semester III									**Total Duration: 28 hrs/week** **Total Marks : 475** **Total Credits: 40**		
Subject	**Teaching Scheme (Hrs)** **Hrs./Week**		**Examination Scheme**						**Examination Scheme** **(Credits)**		**Total Credits**
	L	**P**	**Theory**	**Unit Test**	**Attendance**	**Tutorial/ assignments**	**TW**	**Pract/ Oral**	**TH**	**TW/PR /OR**	
Elective –I	04	02	60	20	10	10	25	25	04	01	05
Elective –II	04	02	60	20	10	10	25	25	04	01	05
**Self-Study Paper-I	* 04	--	60	20	10	10	-	-	04	-	04
Dissertation Stage –I	-	07	-	-	---	--	25	--		21	21
Seminar	-	05	-	-	--	--	25	25	-	05	05
Total	**12**	**16**	**180**	**60**	**30**	**30**	**100**	**75**	**12**	**28**	**40**

Elective – I	**Elective - II**
• Programmable System on chip • Nano electronics • Algorithms for VLSI Design Automation	• ASIC Design • Testing & Verification of VLSI Design • Artificial neural networks

Semester IV									**Total Duration: 14 hrs/week** **Total Marks : 325** **Total Credits: 34**		
Subject	**Teaching Scheme (Hrs)** **Hrs./Week**		**Examination Scheme**						**Examination Scheme** **(Credits)**		**Total Credits**
	L	**P**	**Theory**	**Unit Test**	**Attendance**	**Tutorial/ assignments**	**TW**	**Pract/ Oral**	**TH**	**TW/PR /OR**	
**Self-Study Paper-II	* 04	--	60	20	10	10	-	-	04	-	04
Dissertation Stage –II	-	10	-	-	--	-	150	75		30	30
Total	**04**	**10**	**60**	**20**	**10**	**10**	**150**	**75**	**04**	**30**	**34**

List of Self Study Subjects

Sr. No.	SELF STUDY PAPER- I (SEM-III)	SELF STUDY PAPER- II (SEM-IV)
1	Low power VLSI Design	Genetic algorithms & optimization techniques
2	IC Fabrication Technology	Fuzzy logic systems
3	In-Vehicle Networking	Biomedical Instrumentation
4	Research methodology	Computer aided VLSI Design
5	Intellectual property rights	Human values & professional ethics



M.Tech.(Electronics-VLSI) Sem-III

Bharati Vidyapeeth Deemed University,
College of Engineering, Pune

Elective I- PROGRAMMABLE SYSTEM ON CHIP

TEACHING SCEME

Lectures: 04 Hrs/Week

Practicals:02 Hrs/week

EXAMINATION SCHEME

Duration: 03 Hrs

Theory : 60 Marks

Internal Assessment: 40 Marks

TW&OR:50 Marks

Total Credits: 05

Course prerequisites:
Knowledge of microprocessors and microcontrollers

Course objective:

1. To introduce the students to the Cypress PSoC technology
2. To study the architecture of PSoC
3. To learn interfacing of real world with PSoC

Course Outcomes: Upon Completion of the course, the students will be able to

1. Describe and identify the features of PSoC
2. Design the system for interfacing to the real world.

Contents:

UNIT I (08 hours)

Introduction to PSoC

PSoC Technology, Programmable Routing and Interconnect Configurable Analog and Digital Blocks, CPU Sub System, Families of PSoC (PSoC1, PSoC2, PSoC3,) Difference between PSoC and Conventional MCU.

UNIT II (08 hours)

Introduction to PSoC 3/5

PSoC3/5 architecture-block diagram system wide resources, I/O interfaces, CPU Subsystem, memory organization digital subsystems, analog subsystems

UNIT III (08 hours)

PSoC Design Modules

Cypress PSoC Structure, PSoC Designer Suit, limitations of PSoC improvements of the PSoC, PSoC Subsystem design, PSoC memory management.

UNIT IV (08 hours)

Mixed –Signal Embedded design

Overview of mixed-signal embedded system designs, hardware and software subsystems of mixed-signal architectures, PSoC Hardware components, PSoC software components, PSoC interrupt subsystem, Introduction to PSoC Express, System design using PSoC express**.(8hrs)**

UNIT V (08 hours)

PSoC Components

Universal Digital Blocks (UDB), UDB arrays and digital System Interconnect (DSI),Timer, Counter and PWM,Digital Filter Blocks (DFB),ADC topologies and Circuits Programmable gain amplifiers, Switched capacitor / continuous time, analog routing, flash temperature sensors,DTMF Dialers, Sleep times,UART.12C,SPI,USB,CAN buses.

UNIT VI (08 hours)

System design using PSoC

Interfacing of temperature Sensors and Tachometers, SPI and UART based task communications, Lower Noise Continuous Time Signal Processing with PSoC Data Acquisition and Control System with PSoC, Ultra wide-band RADAR, Serial Bit Receiver with Hardware Manchester Decoder, DTMF Detector, and Ultrasonic Vehicle Parking Assistant, Universal wide-Range Signal Generator.

Text Books:

1. PSoC3, PSoC5 Architecture Technical Reference Manual-Cypress website
2. My First Five PSoC3 Designs (e-book)by Robert Ashby-Cypress website

Reference Books:

1. Designers Guide to the Cypress PSoC by Robert Ashby –Elsevier Publications
2. Introduction to Mixed Signal Embedded Design, Alex Boboli-Springer
3. The Beginners Guide to Using PSoC Express: Mixed –Signal Microcontroller Development Without code by Oliver H.Bailey-Timelines Industries Incorporated,2007
4. PSoC Microcontroller by Fredi Kruger Franzis,2006

Web references

www.cypress.com/go/psoc

www.cypress.com/go/training

www.cypress.com/go/support

www.psocdeveloper.com

Bharati Vidyapeeth Deemed University,
College of Engineering, Pune

Elective I-NANO ELECTRONICS

TEACHING SCHEME

Lectures: 04 Hrs/Week

Practicals: 02 Hrs/Week

EXAMINATION SCHEME

Duration:03 Hrs

Theory: 60 Marks

Internal Assessment: 40 Marks

TW&OR: 50 Marks

Total Credits: 05

Course Prerequisite:

Physics, Basic electronics

Course Objective:

To learn and understand basic and advance concepts of nanoelectronics.

Course Outcomes: On successful completion of this course, students will be able to

1. Understand basic and advanced concepts of nanoelectronic devices
2. Gain knowledge about Nanostructure devices and logic devices.
3. Know the techniques of fabrication and measurement.

Contents:

UNIT I **(08 hours)**

Basics of nanoelectronics

Capabilities of nanoelectronics – physical fundamentals of nanoelectronics – basics of information theory – the tools for micro and nano fabrication – basics of lithographic techniques for Nanoelectronics

UNIT II **(08 hours)**

Quantum electron devices

classical to quantum physics: upcoming electronic devices – electrons in mesoscopic structure – short channel MOS transistor – split gate transistor – electron wave transistor – electron spin transistor – quantum cellular automate – quantum dot array – Principles of Single Electron Transistor (SET) – SET circuit design – comparison between FET and SET circuit design

UNIT III **(08 hours)**

Fabrication and Measurement Techniques

Growth, fabrication, and measurement techniques for nanostructures- Bulk crystal and heterostructure growth- Nanolithography, etching, and other means for fabrication of nanostructures and nanodevices- Techniques for characterization of nanostructures- Spontaneous formation and ordering of nanostructures- Clusters and nanocrystals- Methods of nanotube growth- Chemical and biological methods for nanoscale fabrication- Fabrication of nano-electromechanical systems

UNIT IV **(08 hours)**

Nanostructure Devices -I

Electron transport in semiconductors and nanostructures- Time and length scales of the electrons in solids- Statistics of the electrons in solids and nanostructures- Density of states of electrons in nanostructures- Electron transport in nanostructures-Electrons in traditional low-dimensional structures- Electrons in quantum wells- Electrons in quantum wires- Electrons in quantum dots

UNIT V **(08 hours)**

Nanostructure devices- II

Resonant-tunneling diodes- Potential-effect transistors- Light-emitting diodes and lasers- Nano-electromechanical system devices- Molecular electronics – elementary circuits – flux quantum devices – application of superconducting devices –Strain –oxide nanowire, Nano designs and Nanocontacts – metallic nanostructures

UNIT VI **(08 hours)**

Logic Devices and Applications

Logic Devices-Silicon MOSFETs-Ferroelectric Field Effect Transistors-Quantum Transport Devices Based on Resonant Tunneling-Single-Electron Devices for Logic Applications-Superconductor Digital Electronics-Quantum Computing Using Superconductors-Carbon Nanotubes for Data Processing- Molecular Electronics

Text Books :

1. Karl Goser, Peter Glösekötter, Jan Dienstuhl,“Nanoelectronics and Nanosystems: From Transistors to Molecular and Quantum Devices“, Springer 2004

2. Mick Wilson, Kamali Kannangara, Geoff Smith, Michelle Simmons, Burkhard Raguse,”Nanotechnology: basic science and emerging technologies”, Overseas Press (2005)

Reference Books:

1. Rainer Waser (edition, 2005) ,”Nanoelectronics and Information Technology” ,John Wiley & Sons, Germany.

2. Vladimir V. Mitin, Viatcheslav A. Kochelap, Michael A. Stroscio, “Introduction to Nanoelectronics: Science, Nanotechnology, Engineering, and Applications”, Cambridge University Press 2011

3. Supriyo Datta,“Lessons from Nanoelectronics: A New Perspective on Transport”, World Scientific 2012 6. George W. Hanson,“Fundamentals of Nanoelectronics”, Pearson 2009

4. Korkin, Anatoli; Rosei, Federico (Eds.), “Nanoelectronics and Photonics”,Springer 2008

5. Mircea Dragoman, Daniela Dragoman, “Nanoelectronics: principles and devices”, CRC Press 2006

6. W. R. Fahrner, Nanotechnology and Nan electronics: Materials, Devices, Measurement Techniques (SpringerVerlag Berlin Heidelberg 2005)

7. Mark A. Reed, Takhee Lee,“Molecular nanoelectronics”, American Scientific Publishers 2003

8.. Jaap Hoekstra, “Introduction to Nanoelectronic Single-Electron Circuit Design”, Pan Stanford Publishing 2010

Bharati Vidyapeeth Deemed University,
College of Engineering, Pune

Elective I-ALGORITHMS FOR VLSI DESIGN AUTOMATION

TEACHING SCEME

Lectures: 04 Hrs/Week

Practicals: 02 Hrs/Week

EXAMINATION SCHEME

Duration: 03 Hrs

Theory : 60 Marks

Internal Assessment: 40 Marks

TW&OR:50 Marks

Total Credits: 05

Course Prerequisites:

Analog and Digital VLSI Design, Engineering Mathematics

Course objective:

To introduce the student to the algorithms used for VLSI Design Automation

---

Course Outcomes: After successfully completing the course students will be able to

1. Apply various algorithms for VLSI design.
2. Conceptualize placement, floorplanning and pin assignment.
3. Plan global and detailed routing.
4. Apply concepts of via minimization and compaction

Contents:

UNIT I (08 Hours)

Basic Algorithms

Basic Terminology, Complexity issues, NP- hardness, Graph algorithms, Computational geometry algorithms.

UNIT II (08 Hours)

Partitioning

Problem formulation, Classification of partitioning algorithms, Group migration algorithms, Simulated annealing & evolution, Other partitioning algorithms.

UNIT III (08 Hours)

Placement, Floor Planning and Pin Assignment
Problem formulation, Classification of Placement algorithms, Overview of placement algorithms, Constrain based floor planning, Floor planning algorithms for mixed block and cell design, General and channel pin assignment.

UNIT IV (08 Hours)

Global Routing
Problem formulation, classification of global routing algorithms, Maze routing algorithms, Line probe algorithm, Steiner tree based algorithms, ILP based approaches.

UNIT V (08 Hours)

Detailed Routing
Problem formulation, classification of routing algorithms, single layer routing algorithms, Two layer channel routing algorithm, Three layer channel routing algorithm & switch box routing algorithms.

UNIT VI (08 Hours)

Over The Cell Routing & Via Minimization:
Two layers over the cell routers, Constrained & unconstrained via minimization.
Compaction:
Problem formulation, one-dimensional compaction, Two dimension based compaction, hierarchical compaction.

Text Books/ References:

1. Naveed Shervani, ,"Algorithms for VLSI physical design Automation", Kluwer Academic Publisher, Third edition, 1999.
2. Christophn Meinel & Thorsten Theobold, "Algorithm and Data Structures for VLSI Design", Springer, 1998.
3. Rolf Drechsheler ,"Evolutionary Algorithm for VLSI", Second edition KAP, 1998
4. Trimburger, ,"Introduction to CAD for VLSI", Kluwer Academic publisher, 2002

Bharati Vidyapeeth Deemed University,
College of Engineering, Pune

Elective II -ASIC DESIGN

TEACHING SCEME

Lectures: 04 Hrs/Week

Practicals: 02 Hrs/Week

EXAMINATION SCHEME

Duration: 03 Hrs

Theory : 60 Marks

Internal Assessment: 40 Marks

Total Credits: 05

Course prerequisites:
Digital VLSI Design

Course objective:

The course focuses on the semi custom IC Design and introduces the principles of design logic cells, I/O cells and interconnects architecture, with equal importance given to FPGA and ASIC styles.

Course Outcomes: On successful completion of this course, students will be able to

1. Apply fundamentals of ASIC and its design methods
2. Understand block level abstractions of FPGA and ASIC design
3. Gain knowledge on programmable architectures for ASICs
4. Conceptualize the physical design of ASIC.

Contents:

UNIT-I (08 Hours)

Introduction to ASICS, CMOS Logic and ASIC Library Design
Types of ASICs, Design flow, Combinational Logic Cell, Sequential logic cell, Data path logic cell, Transistors as Resistors, Transistor Parasitic Capacitance, Logical effort.

UNIT-II (08 Hours)

Programmable ASICS, Programmable ASICS Logic Cells and Programmable ASICS I/O Cells
Anti fuse, static RAM , EPROM and EEPROM technology, Actel ACT , Xilinx LCA, Altera FLEX , Altera MAX DC & AC inputs and outputs , Clock & Power inputs, Xilinx I/O blocks.

UNIT-III (08 Hours)

Programmable ASIC Logic Cells
Actel ACT, Xilinx LCA , Xilinx EPLD, Altera MAX 50 00 and 7000 , Altera MAX 9000 , Altera FLEX, Design systems, Logic Synthesis , Half gate ASIC, Schematic entry, Low level design language.

UNIT-IV (08 Hours)

Logic Synthesis, Simulation and Testing
VHDL and logic synthesis, Types of simulation, Boundary scan test, Fault simulation, Automatic test pattern generation.

UNIT-V (08 Hours)

ASIC Floor Planning, Placement and Routing
System partition, FPGA partitioning, Partitioning methods, Floor planning, Placement, Physical design flow, Global routing, Detailed routing

UNIT-VI (08 Hours)

Optimization Algorithms
Planar subset problem(PSP), single layer global routing single layer detailed routing wire length and bend minimization technique, over the cell(OTC) Routing, multichip modules(MCM), Programmable logic arrays, Transistor chaining, Weinberger Arrays, Gate Matrix Layout.

Reference Books:

1. M.J.S.Smith, " Application Specific Integrated Circuits", Pearson,2003
2. Steve Kilts, “Advanced FPGA Design,” Wiley Inter-Science.
3. Roger Woods, John McAllister, Dr. Ying Yi, Gaye Lightbod , “FPGA based Implementation of Signal Processing Systems”, Wiley, 2008
4. Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing ", Mc Graw Hill, 1994.
5. Douglas J. Smith, HDL Chip Design , Madison, AL, USA: Doone Publications, 1996.
6. Jose E. France, Yannis Tsividis, "Design of Analog Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994
7. Farzad Nekoogar and Faranak Nekoogar, “From ASICs to SOCs: A Practical Approach”, Prentice Hall PTR, 2003.

Elective II -TESTING AND VERIFICATION OF VLSI DESIGN

TEACHING SCEME

Lectures: 04 Hrs/Week

Practicals: 02 Hrs/Week

EXAMINATION SCHEME

Duration: 03 Hrs

Theory : 60 Marks

Internal Assessment: 40 Marks

TW&OR:50 Marks

Total Credits: 05

Course prerequisites:
Analog and Digital VLSI Design

Course objective:

To introduce the student to the mathematical and scientific principles based on which systematic test and validation can be carried out on multimillion transistor VLSI design.

Course Outcomes: On successful completion of this course, students will be able to

1. Apply various fault modeling for digital circuits.
2. Test VLSI circuits.
3. Conceptualize Verification process.
4. Plan verification using verification tools.
5. Apply concepts of DFT and BIST.

Contents:

UNIT I (08 Hours)

Introduction to Verification

Importance of verification, Testbench, Human factor, What is being verified, Functional verification approaches, Testing v/s Verification, Verification and design reuse, Cost of verification.

UNIT II (08 Hours)

Verification Tools

Linting Tools, Simulators, Third party models, Waveform viewers, Code coverage.

UNIT III (08 Hours)

Verification Plan

Role of verification plan, Levels of verification, Verification strategies, From specification to features, From features to testcases, From testcases to testbenchs.

UNIT IV (08 Hours)

Basics of Testing and Fault Modeling

Introduction to Testing, Faults in digital circuits, Modeling of faults, Logical Fault Models, Fault
Detection, Fault dominance, Delay fault models.

UNIT V (08 Hours)

Test Generation for Combinational and Sequential Circuits

Test generation for combinational logic circuits, Testable combinational logic circuit design, Test generation for sequential circuits, Design of testable sequential circuits.

UNIT VI (08 Hours)

DFT and BIST

Design for Testability, Ad-hoc design, Scan based design, Built-In-Self-Test.

Text Books/ References:

1. Janick Bergeron ,"Writing Testbenches: Functional Verification of HDL Models", Springer, Second Edition, 2003
2. M.L. Bushnell and V.D. Agrawa,"Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits- l, "Kluwer Academic Publishers, 2002
3. A.L.Crouch ,"Design Test for Digital IC's and Embedded Core Systems", Prentice Hall International, 2002.
4. M.Abramovici, M.A.Breuer and A.D. Friedman ,"Digital systems and Testable Design", Jaico Publishing House, 2002.

Bharati Vidyapeeth Deemed University,
College of Engineering, Pune

Elective II-ARTIFICIAL NEURAL NETWORK

TEACHING SCEME

Lectures: 04 Hrs/Week

Practicals: 02 Hrs/Week

EXAMINATION SCHEME

Duration: 03 Hrs

Theory : 60 Marks

Internal Assessment: 40 Marks

TW&OR:50 Marks

Total Credits: 05

Course prerequisites:

- Basic knowledge of human nervous systems.
- Basic knowledge of mathematical concepts like state-space, Matrix fundamentals.

Course objective:

This course provides in depth knowledge of Artificial Neural Network and role of ANN in different application areas.

Course Outcomes: On successful completion of this course, students will be able to

1 Identify potential use of learning approaches of ANN.
2. Analyze role of perceptron, Adaline & Madeline networks
3. Evaluate different application scenarios of ANN

Contents:

UNIT I (08 Hours)

Introduction and ANN Structure.
Biological neurons and artificial neurons, Model of an ANN, ANN Terminologies, Activation functions used in ANNs, Typical classes of network architectures, Mc-Culloch-Pitts Neuron Model, Learning rules.

UNIT II (08 Hours)

Mathematical Foundations and Learning mechanisms.
Re-visiting vector and matrix algebra, State-space concepts, Concepts of optimization, Error-correction learning, Memory-based learning, Hebbian learning, Competitive learning.

UNIT III (08 Hours)

Single layer perceptrons. Adaline & Madeline Networks

Structure and learning of perceptrons, Pattern classifier - introduction and Bayes' Classifiers, Perceptron as a pattern classifier, Perceptron convergence, Limitations of a perceptrons, Adaline architecture, algorithm, MR-I, MR-II algorithms.

UNIT IV (08 Hours)

Feedforward ANN.

Structures of Multi-layer feedforward networks, Back propagation algorithm, Back propagation - training and convergence, Functional approximation with back propagation, Practical and design issues of back propagation learning. Radial Basis Function Networks, Pattern separability and interpolation, Regularization Theory, Regularization and RBF networks, RBF network design and training, Approximation properties of RBF.

UNIT V (08 Hours)

Competitive Learning and Self organizing ANN

General clustering procedures, Learning Vector Quantization (LVQ), Competitive learning algorithms and architectures, Self organizing feature map, Properties of feature maps, Mexican Net, Hamming Net.

UNIT VI (08 Hours)

Special Networks & Applications of Neural Networks

Support Vector machines**,** Design of an SVM, Examples of SVM, Probabilistic Neural Network, Boltzmann Machine with learning, cognitron, simulated annealing, applications of Neural Networks in bioinformatics, forecasting, healthcare, robotics, pattern recognition.

Text Books/ References:

- Simon Haykin, "Neural Networks: A comprehensive foundation", Second Edition, Pearson Education Asia.
- Satish Kumar, "Neural Networks: A classroom approach", Tata McGraw Hill, 2004.
- Robert J. Schalkoff, "Artificial Neural Networks", McGraw-Hill International Editions, 1997.
- S.N. Sivananadam, “Introduction to Neural Networks using MATLAB”, The McGraw-Hill, 2006.

Bharati Vidyapeeth Deemed University,
College of Engineering, Pune

Self Study Paper I -LOW POWER VLSI DESIGN

TEACHING SCEME

Lectures: 04 Hrs/Week

EXAMINATION SCHEME

Duration: 03 Hrs

Theory : 60 Marks

Internal Assessment: 40 Marks

Total Credits: 04

Course prerequisites:

Analog and Digital VLSI Design

Course objective:

To introduce the student to the concept of low power VLSI design, power estimation and power optimization

---

Course Outcomes:

1. Ability to apply various low power techniques at device and circuit level.
1. Ability to design low power VLSI circuits.
2. Ability to conceptualize low power VLSI basics.
3. Ability to plan low power architectures.
4. Ability to apply concepts of low power design at system level.

Contents:

UNIT I (08 Hours)

Low Power Basics

Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits, Emerging Low power approaches, Physics of power dissipation in CMOS devices.

UNIT II (08 Hours)

Impact of Device & Technology on Low Power

Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

UNIT III (08 Hours)

Low Power Design

Circuit level:
Power consumption in circuits, Flip Flops & Latches design, High capacitance nodes, Low power digital cells library

Logic level:
Gate Reorganization, Signal Gating, Logic Encoding, State Machine Encoding, Pre-Computation Logic

UNIT IV (08 Hours)

Low power Architecture & Systems

Power & performance management, Switching activity reduction, Parallel and Pipeline architecture for low power memory design.

UNIT V (08 Hours)

Low power Clock Distribution

Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co-design of clock network

UNIT VI (08 Hours)

Algorithm & architectural level methodologies

Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation &
synthesis.

Text Books/ References:

1. Gary K. Yeap ,"Practical Low Power Digital VLSI Design", KAP, 2002
2. Rabaey, Pedram ,"Low power design methodologies", Kluwer Academic, 1997
3. Kaushik Roy, Sharat Prasad ,"Low-Power CMOS VLSI Circuit Design",Wiley,2000

Bharati Vidyapeeth Deemed University,
College of Engineering, Pune

Self Study Paper I -IC FABRICATION TECHNOLOGY

TEACHING SCHEME

Lectures: 04 Hrs/Week

EXAMINATION SCHEME

Duration: 03 Hrs

Theory : 60 Marks

Internal Assessment: 40 Marks

Total Credits: 04

Course prerequisites:

Physics, Chemistry

Course objective:

To understand theory and to learn IC Fabrication Technology..

Course Outcomes: On successful completion of this course, students will be able to

1. Conceptualize steps required for IC fabrication.
2. Apply concepts of Oxidation, Lithography , Chemical Vapour Deposition and Metal Film Deposition.

Contents:

UNIT-I (08 Hours)

Environment for VLSI Technology
Basic Fabrication Steps, Concepts of Clean room and safety requirements, Wafer cleaning processes and Wet chemical etching techniques.

UNIT-II (08 Hours)

Oxidation
Kinetics of Silicon dioxide growth for thick, thin and ultrathin films. Oxidation technologies in VLSI and ULSI, High k and Low k dielectrics

UNIT-III (08 Hours)

Lithography
Photolithography, E-beam lithography and newer lithography techniques for VLSI/ULSI.

UNIT-IV (08 Hours)

Chemical Vapour Deposition Techniques
CVD techniques for deposition of polysilicon, silicon dioxide, silicon nitride and metal film

UNIT-V (08 Hours)

Metal Film Deposition
Evaporation and sputtering techniques, Failure mechanisms in metal interconnects Multi-level metallization schemes

UNIT-VI (08 Hours)

Rapid Thermal Processing
PECVD, Plasma etching and RIE techniques; RTP techniques for annealing, growth and deposition of various films for use in ULSI

Reference Books:

1. S.K. Ghandhi, "VLSI Fabrication Principles," John Wiley Inc., New York, 1994(2nd Edition).
2.S.M. Sze (Ed), "VLSI Technology", 2nd Edition, McGraw Hill, 1988.
3.Plummer, Deal , Griffin "Silicon VLSI Technology: Fundamentals, Practice & Modeling" PH,2001.
4.P. VanZant , "Microchip Fabrication", 5th Edition, MH , 2000.

Bharati Vidyapeeth Deemed University,
College of Engineering, Pune

Self Study Paper I -IN-VEHICLE NETWORKING

TEACHING SCEME

Lectures: 04 Hrs/Week

EXAMINATION SCHEME

Duration: 03 Hrs

Theory: 60 Marks

Internal Assessment: 40 Marks

Total Credits: 04

Course prerequisites:

Knowledge of Basic Electronics and Physics

Course objective:

1. To Provide Students with a working of in-vehicle network systems and exposure to aspects of design, development, application issues associated with those systems.

2. To Provide Knowledge in concepts of capture of Sensor data, Storge and exchange of data to obtain remote services.

Course Outcomes: On successful completion of this course, students will be able to

1. Get knowledge in Information –intensive applications that are being enabled for vehicles by a combination of telecommunication computing technology.
2. Develop communications, and navigation/in automotive telemetries.

Contents:

UNIT I (08 hours)

Basics of In-vehicle Networking

Over view of Data communication and networking –need for In-Vehicle networking-layers of OSI reference model –multiplexing and de-multiplexing concepts-vehicles

UNIT II (08 hours)

Networks and Protocols

Over view of general purpose networks and protocols –Ethernet, TCP, UDP, IP, ICMP, ARM, RARP, Over view CAN-Fundamentals-selecting CAN controller-CAN development tools-CAN application areas.

CAN protocol: principles of Data exchange –real time transmission –message frame formats, bit encoding bit physical layer standards

UNIT III (08 hours)

CAN Higher Layer Protocol

Introduction to CAN open-Device net –TTCAN-SAE J1939-overview of CAN open and application in transportation electronics –CAN open standards

UNIT IV (08 hours)

LIN Protocol

LIN standard over view – applications- LIN communication concept message frame-development flow

UNIT V (08 hours)

MOST and Flex Ray

MOST over view –Data rates –data types-topology –application areas –Flex Ray Introduction-network topology –ECUs and bus interfaces –controller host interface and protocol operation controls-media Access Control and frame and Symbol processing –Coding/decoding unit-Flex Ray Scheduling –message processing –wakeup/Startup-applications

UNIT VI (08 hours)

Wireless Systems

Introduction to wireless system –GPS –Setting receivers-Positioning-activating the navigation function –Concept of latitude and grid System-mapping and location technologies-Application.

Reference Books:

1. B.Hoffman-Wellenhof,H.Lichtenegger and J.Collins,"GPS Theory and practice ".4th revised edition, Spriger,Wein New York,1997
2. A.Leick,"GPS satellite Surveying",2edition,John Wiley and Sons, New York, 1995
3. Wireless Systems,W.C.Y.lee,prentice hall Publ. (LBS) -mobile and Wireless design
4. Konrad Etschberger, Controller Area Network, IXXAT Automation August 22, 2001.
5. Olaf Pfeiffer, Andrew Ayre,Christian Keydel,Embedded Networking with CAN and CAN open ,Anna books/Rtc Books,Novenber 1,2003
6. Ronald K Jurgen, Automotive Electronics Handbook, McGraw-Hill Lnc.1999.
7. Dennis Foy,Automotive Telemetric ,Red Hat,2002.

Bharati Vidyapeeth Deemed University,
College of Engineering, Pune

Self Study Paper I -RESEARCH METHODOLOGY

TEACHING SCHEME

Lectures: 04 Hrs/Week

EXAMINATION SCHEME

Duration: 03 Hrs

Theory: 60 Marks

Internal Assessment: 40 Marks

TW & OR : 50 Marks

Total Credits: 04

Course prerequisites:

- Basic knowledge of modeling and simulation.
- Basic knowledge of probability and statistics

Course objective:

This course provides basic knowledge of Research Methodology in different areas.

Course Outcomes: On successful completion of this course, students will be able to

1. Learn research fundamentals like objectives, literature review process.
2. Apply the various methods of modeling and simulation.
3. Apply the probability statistics in the simulation.
4. Write the technical research paper with required presentation.
5. Know about of Information communication technology: e-research, indices, patents, virtual lab etc

---

Contents:

UNIT I (08 Hours)

Research fundamentals

Definition, objectives, motivation, types of research and approaches, research- descriptive, conceptual, theoretical, applied and experimental

UNIT II (08 Hours)

The initial research process

Literature review, research design, assortment of the problem, identification of problem, defining a problem, objective, sub objective and scope, assumptions, validation criteria, research proposal(synopsis)

UNIT III (08 Hours)

Mathematical modeling and simulation

Mathematical modeling – need, techniques and classification, system models –types, static, dynamic, system simulation – why to simulate, technique of simulation, Monte Carlo simulation, types, continuous modeling, discrete model

UNIT IV (08 Hours)

Probability and statistics in simulation

Role of probability and statistics in simulation, statistical distributions, inference about the difference in means, statistical output analysis

UNIT V (08 Hours)

Design of experiment

Strategy of experimentation, types, basic principle, guidelines, need of precision, types of errors

UNIT VI (08Hours)

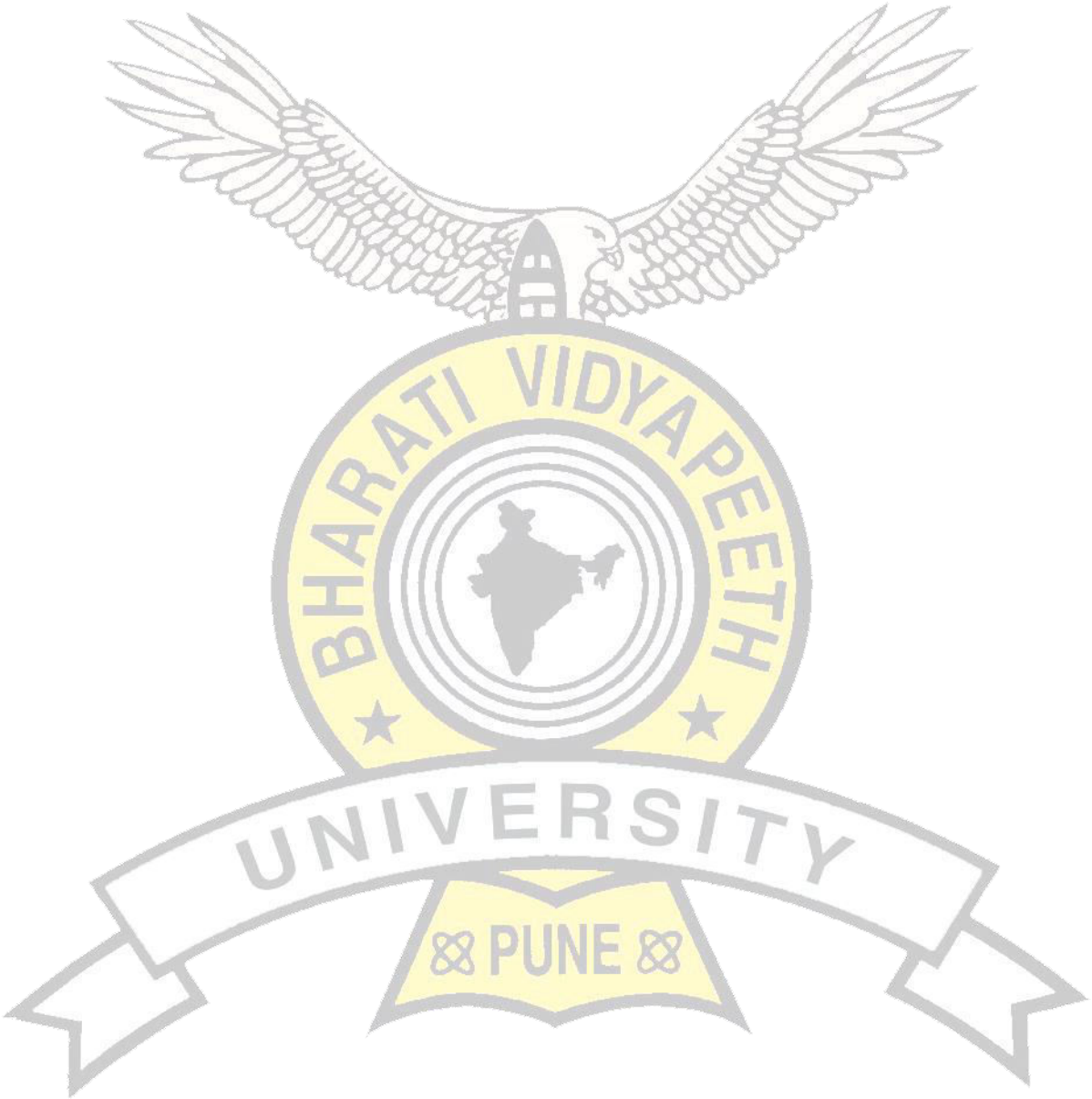
Report writing and presentation of results

Need, report structure, formulation, sections, protocols, graphs, tables, IEEE format, evaluation of report, writing abstract, writing technical paper, Introduction of Information communication technology: e-research, indices, patents, virtual lab, digital lab, ethical issues in research

Reference books:

1. Yogesh Kumar Sing ,"Fundamental of Research Methodology and Statistics" , New Age International Publishers
2. C.R. Kothari, "Research Methodology: Methods and Techniques," New Age International Publishers, 2nd revised Edition
3. Deepak Chawla, Neena Sondhi ,"Research Methodology, Concepts and Cases" , Vikas Publishing House Pvt. Ltd
4. Hamdy A. Taha ,"Simulation Modeling and Simnet" , Prentice Hall International Edition
5. Geoffrey Gorden ,"System Simulation" , Prentice Hall of India Pvt. Ltd.
6. J N Kapur ,"Mathematical Modeling" , Wiley Eastern Ltd

7. Douglas C. Montgomery ,"Design and analysis of Experiments" , Wiley Student Edition, 7th Edition
8. Capt. Dr.Nitin P. Soaje ,"Role of ICT in Doctoral Research "



Bharati Vidyapeeth Deemed University,
College of Engineering, Pune

Self Study Paper I -INTELLECTUAL PROPERTY RIGHTS

TEACHING SCHEME

Lectures: 04 Hrs/Week

EXAMINATION SCHEME

Duration: 03 Hrs

Theory : 60 Marks

Internal Assessment: 40 Marks

TW & OR: 50 Marks

Total Credits: 04

Course objective:

- To introduce fundamental aspects of intellectual property rights to students.
- To provide case studies to demonstrate the application of legal concepts in engineering.

Course Outcomes: On successful completion of this course, students will be able to

- Understand the international intellectual property rights system.
- Use the necessary analytical tools to understand intellectual property in its broader environment

---

Contents:

UNIT I (08 Hours)

Overview of Intellectual Property

Introduction and need for Intellectual Property Rights (IPR),Different categories of IP in instruments, Rational behind Intellectual Property, Rights of the owner of the IP. IPR in India-Genesis & development, International Background of Intellectual Property, some important examples of IPR.

UNIT II (08 Hours)

Patents

Introduction to patents, Concept: Novelty, Utility, Patent document, Granting of patent, Rights of a patent, Drafting of a patent, Filling of a patent, The Indian Patent law,Infringement

UNIT III (08 Hours)

Copyright

Introduction to Copyright, Originality, Works protected under Copyright Law, Authorship and Ownership

UNIT IV (08 Hours)

Trademarks

Introduction, Rights of trademark, Need for protection of trademarks, Types of trademarks, Registration of trademarks, Rights of Registered Trademark Owners, Infringement of trademarks

UNIT V (08 Hours)

Acquisition & maintenance of Intellectual Property Rights

Introduction to Acquisition & maintenance of Intellectual Property Rights,Intellectual property offices(IPOs),Costs-Patents,costs-Trademark,Costs-Copyright

UNIT VI (08 Hours)

Enforcement of Intellectual Property Rights

Introduction to Enforcement of Intellectual Property and Global economy. The knowledge of economy & IP, valuation & accounting of Intangible assets, Management of IP in knowledge economy.

Text books/Reference

1) W.R. Cornish, 'Intellectual Property', Sweet & Maxwell, London (2000)

2) N.S. Gopalakrishnan & T.G. Agitha, 'Principles of Intellectual Property' Eastern Book Company, Lucknow.

3) P. Narayana, 'Patent Law', Wadhwa Publication.

4) V. V. Sopale, 'Managing Intellectual Property: The Strategic Importance', Second edition, PHI.

M.Tech.(Electronics-VLSI) Sem-IV

Bharati Vidyapeeth Deemed University,
College of Engineering, Pune

Self Study Paper II- GENETIC ALGORITHMS FOR VLSI DESIGN

TEACHING SCEME

Lectures: 04 Hrs/Week

EXAMINATION SCHEME

Duration: 03 Hrs

Theory: 60 Marks

Internal Assessment: 40 Marks

TW & OR: 50 Marks

Total Credits: 04

Course prerequisites:

Analog and Digital VLSI Design

Course objective:

To introduce the student to the concept of Genetic Algorithm for VLSI

Course Outcomes:

1. Ability to apply Genetic Algorithm for VLSI Design.
2. Ability to optimize VLSI Design through algorithm.
3. Ability to conceptualize VLSI design flow through Genetic Algorithm .

Contents:

UNIT I (8 hours)

VLSI Design

Design Methodology and Hardware Implementation Methodologies, Digital ASIC Implementation

UNIT II (8 hours)

Genetic Algorithms

Components of a GA Based Optimization Engine, Individual Encoding, Fitness of an Individual, Selection Mechanism Genetic Operators, Crossover Operators, Uniform Crossover, Elitism in Genetic Algorithms, Multi-Objective Genetic Algorithms

UNIT III (8 hours)

Multi-Objective Genetic Floorplanning For Vlsi Asics

Multi-objective Optimization, Floor planning and Floor planning Using Sequence Pair Representation, Conversion from a Floor plan to a Sequence Pair, Conversion from a Sequence Pair to a Floor plan

UNIT IV (8 hours)

FPGA Based Genetic Algorithm

Pseudo-Random Number Generation and GA Performance, Basics of Evolvable Hardware, FPGA Based Genetic Algorithm, Implementation and Interfacing, Design Considerations for ASIC Implementation, RT-Level Simulations, Runtime Comparison of Implemented design.

UNIT V (8 hours)

Power Estimation

Application of GA-Standard cell placement-GA for ATG-problem encoding- fitness function-GA vs Conventional algorithm

UNIT VI (8 hours)

Hybrid Genetic

Genetic encoding-local improvement-WDFR-Comparison of Cas-Standard cell placement-GASP algorithm-unified algorithm.

Text Books

1. Pinaki Mazumder,E.MRudnick,"Genetic Algorithm for VLSI Design,Layout and test Automation", Prentice Hall,1998.

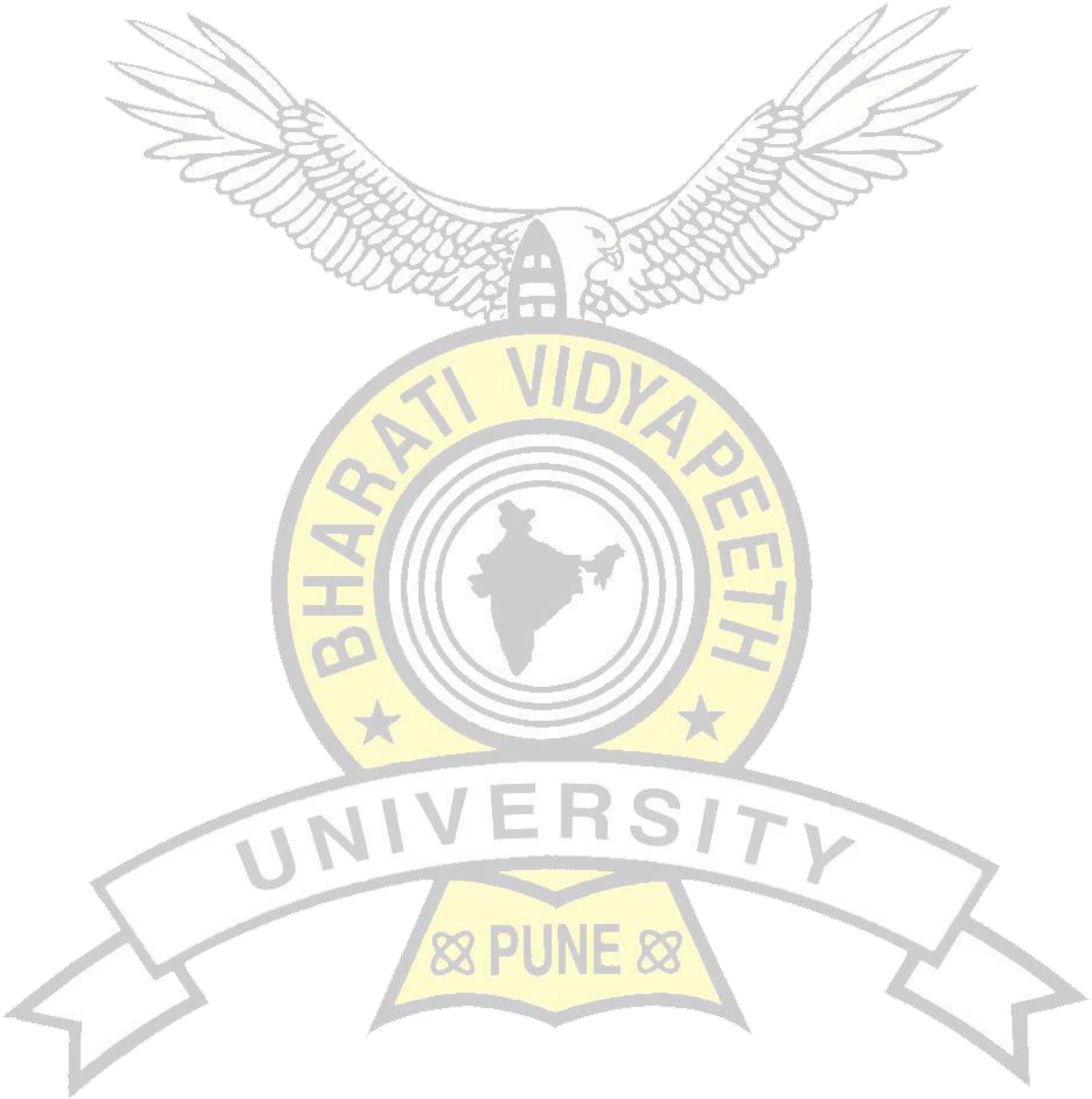
References :

1. Randy L. Haupt, Sue Ellen Haupt, "Practical Genetic Algorithms" Wiley – Interscience,1977.

2. Ricardo Sal Zebulum, Macro Aurelio Pacheco, Marley Maria B.R. Vellasco, Marley Maria Bernard Vellasco "Evolution Electronics: Automatic Design of electronic

Circuits and Systems Genetic Algorithms", CRC press, 1st Edition Dec 2001.

3. John R.Koza, Forrest H.Bennett III, David Andre , Morgan Kufmann, "Genetic Programming Automatic programming and Automatic Circuit Synthesis", 1st Edition , May 1999.



Bharati Vidyapeeth Deemed University,
College of Engineering, Pune

Self-Study Paper II: FUZZY LOGIC SYSTEMS

TEACHING SCHEME

Lectures: 04 Hrs/Week

EXAMINATION SCHEME

Duration: 03 Hrs

Theory: 60 Marks

Internal Assessment: 40 Marks

Total Credits: 04

Course prerequisites:

- Basic knowledge of set & probability theory.
- Basic knowledge of prepositional logic & control systems

Course objective:

This course provides in depth knowledge of Fuzzy Logic and role of Fuzzy Logic systems in different application areas.

Course Outcomes: On successful completion of this course, students will be able to

1. Analyze basic concepts of fuzzy sets, fuzzy relation and fuzzy arithmetic.
2. Identify potential use of fuzzy logic controller in different applications.
3. Evaluate fuzzy logic systems with fuzzy classification, fuzzy pattern recognition and hybrid systems.

Contents:

UNIT I (08 Hours)

Classical Sets and Fuzzy Sets

Crisp Sets: An Overview, Fuzzy Sets: Basic Types, Fuzzy Sets: Basic Concepts, Characteristics and Significance of the Paradigm Shift, Additional Properties of alpha Cuts, representations of Fuzzy Sets, Extension Principle for Fuzzy Sets, Types of Operations, Fuzzy complements, Fuzzy Intersections: t-Norms, Fuzzy Unions: t-Conorms, Multivalued Logic, Fuzzy Propositions, Fuzzy Quantifiers.

UNIT II (08 Hours)

Classical Relations and Fuzzy Relations

Cartesian Product ,crisp relations, operations on crisp Relations, properties of crisp relations, composition, Fuzzy Relations, operations on fuzzy relations, properties of fuzzy relations, Fuzzy Tolerance and Equivalence Relations, Fuzzy Compatibility Relations, Fuzzy Ordering Relations.

UNIT III (08 Hours)

Fuzzy Arithmetic, Fuzzification and Defuzzification

Fuzzy Numbers, Linguistic Variables, Arithmetic Operations on intervals, Arithmetic Operations on Fuzzy Numbers, Lattice of Fuzzy Numbers, Fuzzy Equations, Fuzzification, Defuzzification to Crisp Sets, λ-Cuts for Fuzzy Relations, Defuzzification to Scalars.

UNIT IV (08 Hours)

Fuzzy Systems

Conventional Control Systems, Analysis, Design, PID Control, Fuzzy Logic Controller (FLC), Design, Defuzzification, Analysis, Simplified Examples of Applications- Washing machine, Vacuum cleaner. Fuzzy Control System Design, Aircraft Landing Control Problem, Fuzzy Engineering Process Control, Fuzzy Statistical Process Control. Fuzzy Neural Networks, Fuzzy Automata.

UNIT V (08 Hours)

Fuzzy Classification & Fuzzy Pattern Recognition

Classification by Equivalence Relations, Cluster Analysis, Cluster Validity, *c*-Means Clustering, Hard *c*-Means (HCM), Fuzzy *c*-Means (FCM), Fuzzy *c*-Means Algorithm, Classification Metric, Hardening the Fuzzy *c*-Partition, Similarity Relations from Clustering, Feature Analysis, Partitions of the Feature Space, Single-Sample Identification, Multifeature Pattern Recognition.

UNIT VI (08 Hours)

Hybrid Systems & Applications of Fuzzy Logic

Hybrid Systems, Fuzzy Neuron, Multilayer FNN Architectures, Fuzzy ART, Fuzzy ARTMAP Neural Fuzzy Systems, economics application, civil & industrial applications, Fuzzy Systems and Genetic Algorithms, Fuzzy Regression, Interpersonal Communication.

Text Books/ References:

1. Timothy Ross, “Fuzzy Logic with Engineering Applications", Third Edition, Wiley publication.
2. George J. Klir & Bo Yuan, “Fuzzy Sets & Fuzzy Logic Theory & Applications”, Prentice Hall India, 2007.
3. Ahmad M. Ibrahim “Fuzzy Logic for Embedded Systems Applications” 2003, Elsevier Science.

Bharati Vidyapeeth Deemed University,
College of Engineering, Pune

Self-Study Paper II: BIOMEDICAL INSTRUMENTATION

TEACHING SCHEME

Lectures: 04 Hrs/Week

EXAMINATION SCHEME

Duration: 03 Hrs

Theory: 60 Marks

Internal Assessment: 40 Marks

Total Credits: 04

Course prerequisites:

- Knowledge of basic cell structure, organs and systems in the human body

---

Course objective:

1. To make student understand different body systems.
2. To introduce amplifiers in order to design ECG Preamplifier system to pick up ECG waveform from the body.
3. To introduce various types of blood pressure monitoring and pulse oxymetry techniques.
4. To make student understand the importance of respiratory organs and parameters.
5. To make student understand various types of clinical lab equipments and its applications.
6. To introduce importance of electrosurgical equipment and electrodes used for electrosurgical

---

Course Outcomes: On successful completion of this course, students will be able to

1. Classify different body systems with their functions.
2. Design ECG preamplifier system to pick up ECG waveform from the body.
3. Categorize various pressure transducers as well as measurement techniques used for blood pressure monitoring.
4. Describe respiratory system organs, parameters and respiratory transducers.
5. Describe clinical equipments used in the pathology lab for blood test and analysis.
6. Classify various electrodes and techniques used for surgery.

Contents

UNIT I (08 hours)

Human Body System

Human body as a uniquely adaptable organism , Overview of Different systems

UNIT II (08 hours)

Amplifier Systems for ECG

Introduction to amplifiers in biomedical electronics,ECG wave form,Standard lead system,ECG Preamplifier.

UNIT III (08 hours)

Blood Pressure and Blood Flow Measurements

Physiological pressures, Blood pressure measurements, Pressure transducers, pulse oximetry

UNIT IV (08 hours)

Respiratory System Measurements

Introduction to human respiratory system,organs of Respiration,Parameters of respiration,Respiratory transducers, plethysmography.

UNIT V (08 hours)

Clinical Laboratory Equipments

Blood components, overview of Laboratory measurements,Blood gas Analyzer,Blood cell counters,Spectrophotometer,Blood Tests and analyzers.

UNIT VI (08 hours)

Electrosurgical Equipments

Introduction to Electrosurgical Unit ,electro surgery circuits, Electro surgery safety, Patients safety

Text Books:

1.Joseph.J.Carr and John.M.Brown, "Introduction to Biomedical Equipment Technology",Pearson Education.

References:

1.Arthur C Guyton, "Medical Physiology", Prism Book.

2.Leslie Cromwell,Fred.J.Weibel,"Biomedical Instrumentation and Measurements", PHI.

Self-Study Paper II: COMPUTER AIDED VLSI DESIGN

TEACHING SCHEME

Lectures: 04 Hrs/Week

EXAMINATION SCHEME

Duration: 03 Hrs

Theory: 60 Marks

Internal Assessment: 40 Marks

Total Credits: 04

Course prerequisites:

VLSI Design

Course objective:

The course will introduce CAD tools required for VLSI.

Course Outcomes:

On successful completion of this course, students will effectively utilize various CAD tools for VLSI design.

Contents

UNIT I
Digital Design and Design Environments: (08 hours)

Design, Hierarchy, Views, Connectivity, Spatial Dimensionality, Introduction of Design Environments, System Level, Algorithm Level, Component Level, Layout Level

UNIT II
Representation: (08 hours)

Introduction, General Issues of Representation, Hierarchy Representation, View Representation, Connectivity Representation, Geometry Representation.

UNIT III
Synthesis Tools: (08 hours)

Introduction, Cell Contents Generation and Manipulation, Generators of Layout outside the Cells, Cells and Their Environment, Silicon Compilers, Post layout Generators,

UNIT IV
Static Analysis Tools, Dynamic Analysis Tools: (08 hours)

Node Extraction, Geometrical Rule Checker, Electrical Rule Checker, Verification, Circuit–Level Simulators, Logic-Level Simulators, Functional and Behavioral Simulation Issues, Event Driven and Hardware Simulation

UNIT V
Output of Design Aids and Programmability: (08 hours)
Introduction, Circuit Boards, Integrated Circuits, Implementation Issues, Imperative Programming, Declarative Programming, Hierarchy.

UNIT VI
Graphics and Human Engineering: (08 hours)
Introduction, Display Graphics, Hardcopy Graphics, Input Devices, Task and User Modeling, Information Display, Command Language Feedback.

Book:

1. M.J.S. Smith. Application-Specific Integrated Circuits. Addison Wesley.

Self-Study Paper II: HUMAN VALUES & PROFESSIONAL ETHICS

TEACHING SCHEME

Lectures: 04 Hrs/Week

EXAMINATION SCHEME

Duration: 03 Hrs

Theory: 60 Marks

Internal Assessment: 40 Marks

Total Credits: 04

Course prerequisites:

- Listening skills for academic and professional purposes.
- Ability to speak effectively in English in real-life situations.

Course objective:

1. To create awareness on engineering ethics and human values
2. To understand social responsibility of an engineer
3. To appreciate ethical dilemma while discharging duties in professional life

---

Course Outcomes: On successful completion of this course, students will be able to

1. Familiar with the ethical issue and professional issue in the engineering profession.
2. Familiar with social impact of decision and the action of participants in the engineering profession

---

Contents

UNIT I (08 Hours)

Human Values

Morals, Values and Ethics - Integrity, - Work Ethics - Service Learning - Civic Virtue - Respect for others - Living Peacefully - Caring - sharing - Honesty - Courage - Valuing Time- Cooperation - Commitment - Empathy – Self-Confidence - Character - spirituality

UNIT II (08 Hours)

Engineering Ethics

Senses of engineering ethics - Variety of Moral Issues - Types of inquiry - Moral Dilemmas Moral Autonomy - Kohlberg's Theory - Gilligan's Theory - Consensus and Controversy -

Models of Professional Roles - Theories about Right Action - Self-Interest - Customs and Religion .

UNIT III (08 Hours)

Safety, Responsibilities and Rights

Safety and Risk - Assessment of safety and Risk - Risk Benefit Analysis and Reducing Risk - The Three Mile Island. And Chernobyl Case Studies. Collegiality and Loyalty - Respect for Authority - Collective Bargaining - Confidentiality - Conflicts of Interest - Occupational Crime - Whistle Blowing - Professional Rights – Employee Rights - Intellectual Property Rights (IPR) – Discrimination

UNIT IV (08 Hours)

Global Issues

Multinational Corporations - Environmental Ethics - Computer Ethics - Weapons Development - Engineers as Managers - Consulting Engineers - Engineers as Expert Witnesses and Advisors - Sample Code of Ethics of ASME, ASCE, IEEE, Institution of Engineers (India), etc.

UNIT V (08 Hours)

Engineer's responsibility for safety

Collegiality and loyalty-respect of authority-collective bargaining-confidentiality-conflicts of interest-occupational crime- professional rights-employee rights-Intellectual property rights(IPR).

UNIT VI (08 Hours)

Engineering as social Experimentation

Engineering as social experimentation-engineers as responsible experimenters-codes of ethics-a balanced outlook on law- the challenger case study

Text Books/ References:

- Bayles, M.D.: Professional Ethics, California: Wadsworth Publishing Company, 1981.
- Koehn, D.: The Ground of Professional Ethics, Routledge, 1995.
- R.S. Naagarazan, A Text Book of Professional Ethics & Human Values, New Age
- International, 2006 . Mike Martin and Ronald Schinzinger, Ethics in Engineering",McGraw-Hill,New YORK1996
- Camenisch, P.F.: Grounding Professional Ethics in a Pluralistic Society, N.Y.: Haven Publications, 1983.
- Wuest, D.E. : Professional Ethics and Social Responsibility, Rowman & Littlefield, 1994.